Fusion Test System

VX 250/125 Digital Hardware

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Introduction 1

Overview

The Digital Subsystem hardware delivers test patterns to the device under test (DUT), compares the DUT's response to the expected results, and logs the test results. Multiple DUTs can be simultaneously tested on one test head. The Fusion HF tester supports a maximum of 1024 digital tester channels.

Two digital modes, VX125 and VX250, are available for the control and execution of test patterns.

The Low Speed operation of the Digital Subsystem interprets the test pattern and the expected results, and records test data. The test vectors (test program) provides the information to interpret.

The High Speed operation executes the test. Specified patterns (waveforms, timing, voltage and current levels) are delivered to the DUT. The response of the DUT are compared to the expected results and evaluated as pass/fail. The test results are returned to the tester mainframe for processing.

The following block diagram, Figure 1.1, shows a functional outline of the Digital Subsystem.

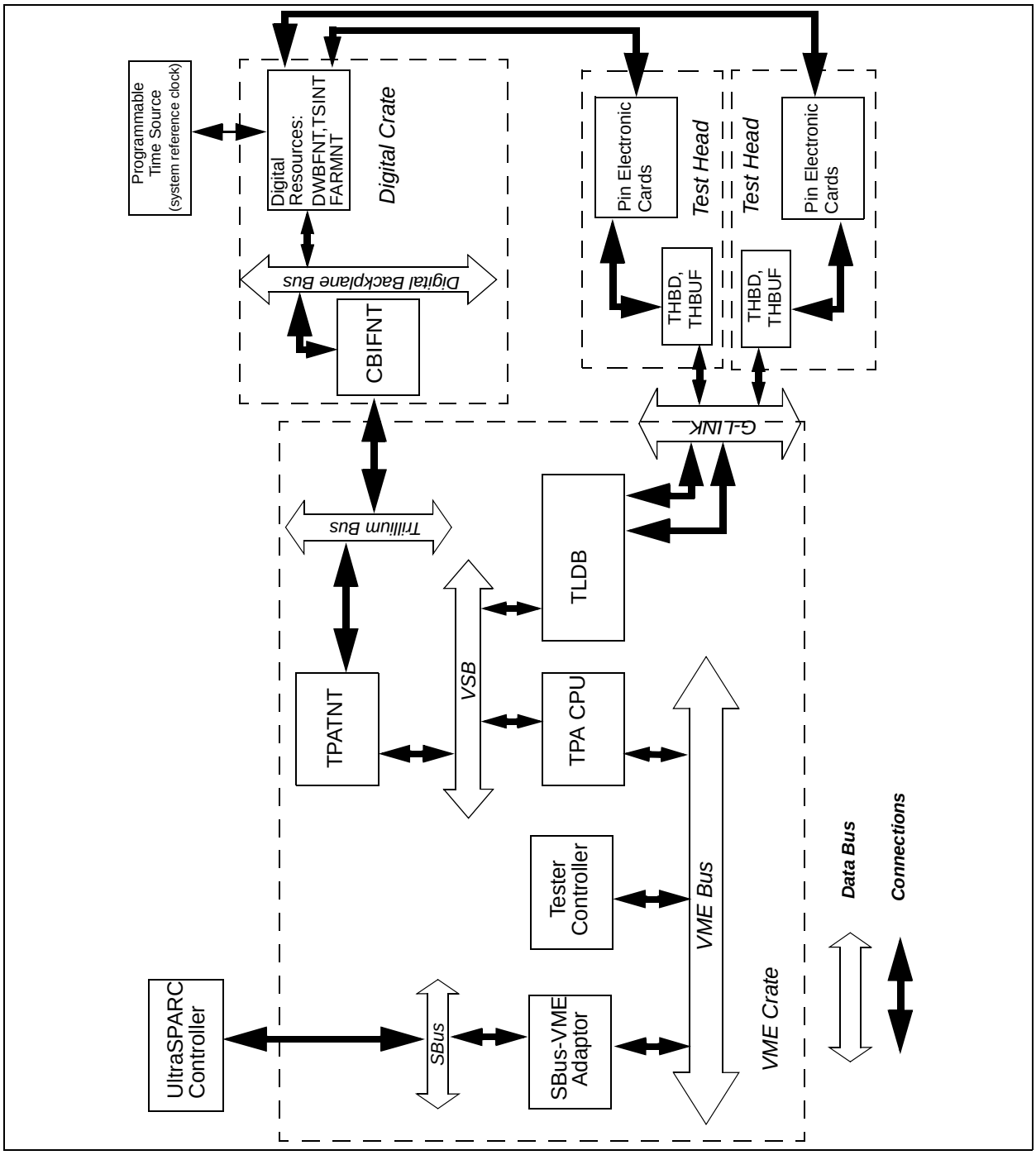


Figure 1.1: Digital Subsystem Hardware, Block Diagram

Although two test heads can be connected to one tester mainframe, only one test head can perform test functions. The operation of the test heads can alternate; the test heads can not execute tests simultaneously.

Digital Modes

Two digital modes are available for the Fusion HF tester: VX250 and VX125. These modes affect the delivery of test patterns to the DUT: speed, available waveform patterns, depth of data pattern memory (DPM).

If VX250 is installed in the tester, both VX125 and VX250 are available: either VX125 or VX250, or both VX125 and VX250 can operate. If VX125 is installed, only VX125 can function.

Dual-Channel mode is available for VX125 and VX250. Dual-Channel mode doubles the number of events per cycle. However, the number of available test channels is reduced.

Timing generators control the number of events per cycle.

Timing Generators

Timing generators control the events of test patterns. There are four independent timing generators per test channel, TG1–TG4. Each timing generator has a 4ns re-trigger time. In the VX125 mode this allows four events per period. In the VX250 mode, the timing generators are paired, which allows eight events per period.

The timing generators are located on the FARMNT boards in the Digital Crate.

Dual-Channel Mode

Dual-Channel mode doubles the amount of events that can occur per period: eight events instead of four. In Dual-Channel mode, the timing markers of two test channels are combined to function with one test channel. Test channel(n) is combined with test channel(n+1): channel 0 can be paired with channel 1, channel 2 with channel 3, and so on.

Each pair of test channels can be programmed independently: drive and compare functions are controlled separately.

When the test channels paired in Dual-Channel mode, the number of available test channels is reduced by one half: One of the paired channels is unavailable.

Dual-Channel Mode is available for VX125 and VX250.

VX125 Digital Mode

VX125 digital mode allows 125MHz bidirectional test rates, and a multiplex mode that doubles the rate to 250MHz.

In VX125, the Control Pattern Memory (CPM) functions with 6 bits, which provides 64 pattern waveforms for selection per test vector. The pattern waveforms are segments of the signals that are delivered through the test channels to the DUT.

The standard memory depth of the data pattern memory (DPM) is 8Mbytes. An available option, Extended DPM, increases the memory to 16Mbytes.

VX250 Digital Mode

The VX250 digital mode allows 250MHz test rates. In the VX250 mode of operation, three bits are available for selecting eight different waveforms through the Control Pattern Memory (CPM).

In VX250, the rate is increased to 250MHz by splitting the four timing generators to two pairs. This reduces the re-trigger time from 4ns to 2ns, and creates two cycles in which two events occur per period. Effectively, one cycle is split to two half-cycles.

VX250 allows the operation of VX125: either separately, or mixed with VX250.

The standard memory depth for the DPM is 16MBytes. Extended Memory DPM provides 32MBytes.

Shared DPM Memory

When VX125 and VX250 modes are both operating, DPM memory is shared. Table 1.1 shows examples of how DPM memory can be divided between VX125 and VX250.

Table 1.1: 8 Mbyte DPM Memory Allocation

Standard memory allocated to VX125	Standard memory allocated to VX250	Extended memory allocated to VX125	Extended memory allocated to VX250
8 Mbytes	0 bytes	16 Mbytes	0 bytes
4 Mbytes	8 Mbytes	8 Mbytes	16 Mbytes
2 Mbytes	12 Mbytes	4 Mbytes	24 Mbytes
0 bytes	16 Mbytes	0 bytes	32 Mbytes

Bus Interface 2

Introduction

A bus is a transmission path on which signals are dropped off or picked up by every printed circuit board that is connected to the path. Only the boards addressed by the signals respond; the other boards ignore the signals.

Each board has a unique address, which enables a board to recognize the signals that are delivered to it.

This section describes the buses and related printed circuit boards:

NOTE This chapter provides an overview of the interaction of the digital boards through the Trillium Bus, and G-Link. For detailed information about enVision++, refer to the online manual. For detailed information about registers, refer to Register Data Base Utility (RDBU).

Trillium Bus

The Trillium bus carries analog and digital bus traffic. The allotted address space of one Trillium Bus supports 256 test channels. To handle 1024 test channels, the Fusion HF tester can be configured with four Trillium buses.

To run tests, and collect and analyze results, the Trillium Bus enables communication with boards in the VME Crate and the Digital Crates. The following boards are connected to the Trillium Bus:

- Test Program Accelerator NT (TPAT2A), VME Crate
- Bus Interface Boards NT (CBIFNT), Digital Crate

Trillium Bus Read/Write Cycles

The Trillium Bus enables the TPAT2A to communicate with the tester through read cycles (receive) and write cycles (transmit). This bus has a 16 bit address field and a 32 bit data field. The address and control signals are unidirectional signals, and the data signals are bi-directional.

The TPAT2A board controls the timing of each bus cycle on the Trillium Bus. For bus transactions, the Trillium Bus uses the control signals that define read and write cycles, and control pointer incrementing as a function of the bus cycle.

Internal to each of the digital backplanes, the Trillium Bus supports up to four interrupt lines. However, at this time, the interrupt lines are not used.

Bus Timing for Registers

To accommodate the timing required per register, the TPAT2A adjusts the timing of each bus cycle per register address.

NOTE For the digital subsystem to work correctly, it is important to leave the timing set as is: Do not modify TPAT2A buscycle timing.

Digital Crate Read/Write Cycles

Through the TPAT2A in the VME CRATE, data is transferred to the Digital Crate through normal mode: read/write. **Figure 1.1 on page 1-2** shows a block diagram of the Digital Subsystem.

NOTE The Trillium Bus does not support direct memory access (DMA).

Read Cycle

The READ signal tells the CBIFNT board when a bus cycle is a read cycle. READ is a logic level only: The rising and falling edges of the signal are not used for clocking.

When a read cycle begins, the data bus portion of the Trillium Bus switches directions: Data is driven data back to the TPAT2A.

During the read cycle, the register that was selected drives data back on the data bus to the TPAT2A. The register continues to drive valid data on the bus until the read signal goes false.

At the end of the read cycle, the direction of the data bus switches over to write.

Figure 2.1 on page 2-4 shows the Trillium bus signals that are active during the normal read cycle.

The CBIFNT board is described in Buffer Interface NT (CBIFNT) on page 2-28.

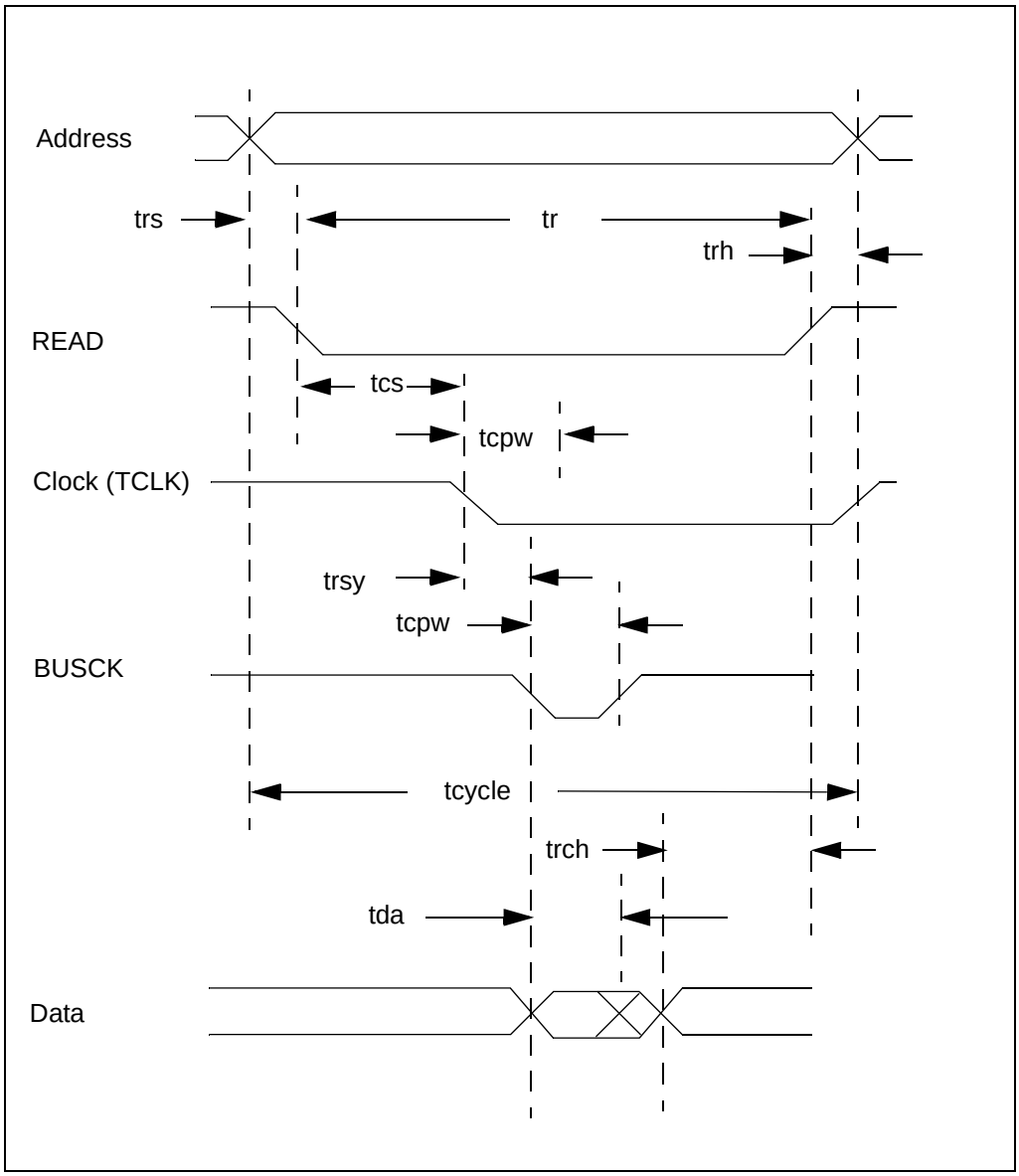


Figure 2.1: Digital Crate Read Cycle, Normal Mode

Bus Clock (BUSCK). BUSCK is synchronized to the TSINT board in the Digital Crate.

TCLK. TCLK is synchronized to the TPAT2A board in the VME Crate, and to the CBIFNT board in the Digital Crate.

Table 2.1 describes the timing of the signals shown in Figure 2.1 on page 2-4.

Table 2.1: Digital Crate Read Cycle, Normal Mode

Signal TIming	Description
trs	The timing from the transition of the Address to the Read signal going true. (One default PSCLK period.)
tr	The width of the Read signal, which is based on the following: n The time it takes for the address to be stable before TCLK can occur (tcs) n The TCLK synchronization time (trsy) n The time its takes for registers that are accessed via a state machine to present their data on the bus (tda) n The time it takes the returning data to the TPAT2A to stabilize at the TPAT2A: Approximately the same as the address stabilization time (tcs), and one PSCLK period between the edge that clocks the data into the TPAT2A and the end of the read cycle.
trh	The timing from the Read signal going false to the loss of valid Address and Data. (One default PSCLK period.)
tcs	The time between Read going true and the leading edge of the Clock (TCLK). This allows time for the address to become stable on the Digital Backplane.
tcpw	The width of the BUSCK. (Two default PSCLK periods.)
trsy	The delay between the TCLK provided by the TPAT2A and the delayed TCLK (BUSCK), which is used by the boards in the digital crate. This delay is caused by the process of synchronizing the TCLK to the PSCLK.
tcycle	The width of the entire bus cycle.
trch	The timing from the trailing edge of RCLK to the trailing edge of the Read signal.(One default PSCLK period.)
tda	The time after the leading edge of TCLK: The register data being output for reading is valid.

Write Cycle, Normal Mode

The Write signal tells the bus interface boards that the bus cycle is a write cycle. This signal is a logic level: the edges of the signal are not used for clocking.

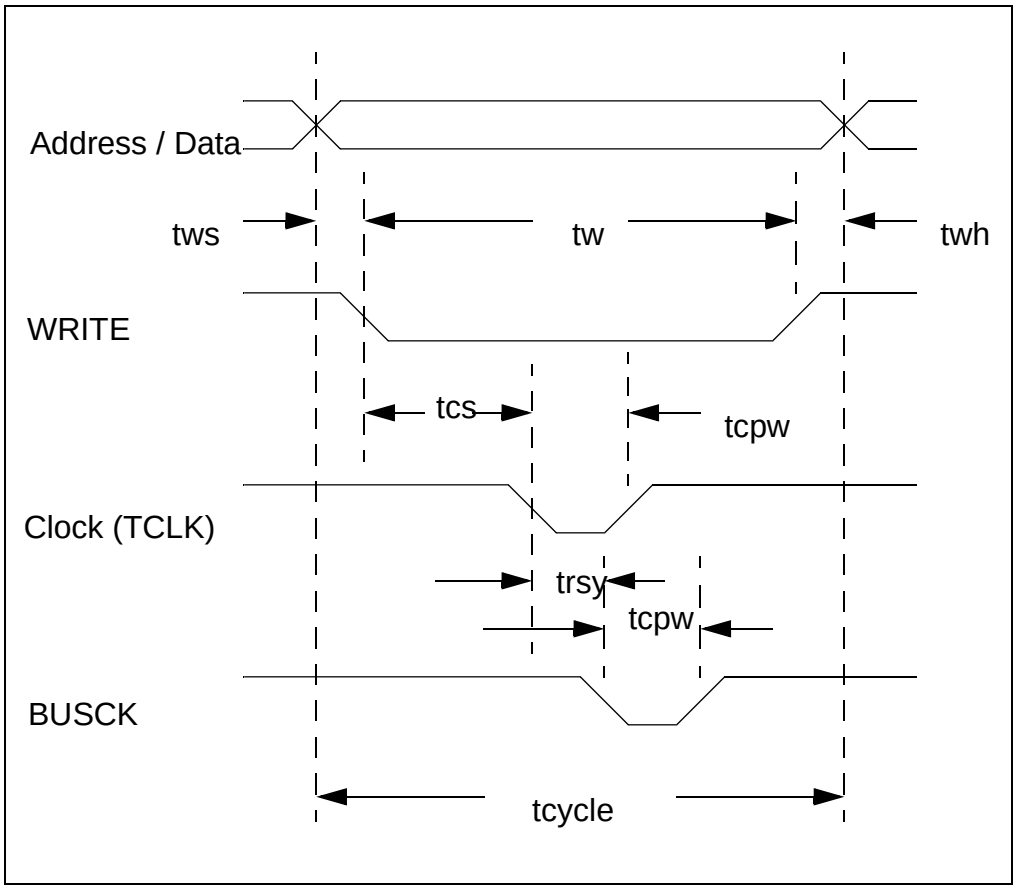


Figure 2.2: Digital Crate Write Cycle, Normal Mode

TCLK. The leading edge of the TCLK signal clocks data into registers.

If a state machine is used to perform the write, the rising edge of TCLK latches the data into a "hold" register while the state machine writes that data to the specified register.

BUSCK. The trailing edge of BUSCK is used to cause specified pointer autoincrements.

When the state machine is used for the write cycle, the state machine may be used to postpone the actual autoincrement event.

Table 2.2 describes the timing of the signals illustrated in Figure 2.2 on page 2-6.

Table 2.2: Digital Crate Write Cycle, Normal Mode

Signal	Table 2.3: Description
tws	The timing from the transition of the Address and Data to the Write signal going true. (One default PSCLK period.)
tw	The width of the Write signal.
twh	The timing from the Write signal going false to the loss of valid Address and Data. (One default PSCLK period.)
tcs	The time between Write going true and the leading edge of the Clock (TCLK). This time is required to give adequate time for the address and data to become stable on the Digital Backplane.
tcpw	The width of the BUSCK. (Two default PSCLK periods.)
trsy	The delay between the TCLK provided by the TPAT2A and the delayed TCLK (BUSCK) used by the boards in the digital crate. This delay is caused by the process of synchronizing the TCLK to the PSCLK.
tcycle	The width of the entire bus cycle.

Daisy Chain

To support 1024 test channels, four CBIFNT boards are “daisy-chained.” One CBIFNT supports 256 test channels.

Signal Input/Output

Table 2.4 on page 2-7 ,Table 2.5 on page 2-8, and Table 2.6 on page 2-9 list the pinout for the address and data bus connectors on the input side of the CBIFNT board (data flowing from TPAT2A to the CBIFNT board).

Table 2.7 on page 2-10 through list the pinout for the address and data bus connectors on the output side of the CBIFNT board (data flowing from one CBIFNT board to the next CBIFNT board).

Table 2.4 lists the pinout of connector BJ01.

Table 2.4: Connector BJ01

Pin Number	Signal	Pin Number	Signal
01	GND	02	GND
03	AIN02	04	AIN02/

Table 2.4: Connector BJ01 (Continued)

Pin Number	Signal	Pin Number	Signal
05	AIN03	06	AIN03/
07	AIN04	08	AIN04/
09	AIN05	10	AIN05/
11	AIN06	12	AIN06/
13	AIN07	14	AIN07/
15	AIN08	16	AIN08/
17	AIN09	18	AIN09/
19	AIN10	20	AIN10/
21	AIN11	22	AIN11/
23	AIN12	24	AIN12/
25	AIN13	26	AIN13/
27	AIN14	28	AIN14/
29	AIN15	30	AIN15/
31	BSYIN	32	BSYIN/
33	CLRIN	34	CLRIN/
35	WRIN	36	WRIN/
37	RDIN	38	RDIN/
39	CLKIN	40	CLKIN/
41	XECIN	42	XECIN/
43	HD2IN	44	HD2IN/
45	HD1IN	46	HD1IN/
47	DMAIN	48	DMAIN/
49	SCKIN	50	SCKIN/

Table 2.5 lists the pinout of connector BJ02.

Table 2.5: Connector BJ02

Pin Number	Signal	Pin Number	Signal
01	GND	02	GND
03		04	
05		06	

Table 2.5: Connector BJ02 (Continued)

Pin Number	Signal	Pin Number	Signal
07		08	
09		10	
11	AIN17/	12	AIN17
13	AIN16/	14	AIN16
15	ANSLIN/	16	ANSLIN
17	SPBJ20/	18	SPBJ20
19	DIN15/	20	DIN15
21	DIN14/	22	DIN14
23	DIN13/	24	DIN13
25	DIN12/	26	DIN12
27	DIN11/	28	DIN11
29	DIN10/	30	DIN10
31	DIN09/	32	DIN09
33	DIN08/	34	DIN08
35	DIN07/	36	DIN07
37	DIN06/	38	DIN06
39	DIN05/	40	DIN05
41	DIN04/	42	DIN04
43	DIN03/	44	DIN03
45	DIN02/	46	DIN02
47	DIN01/	48	DIN01
49	DIN00/	50	DIN00

Table 2.6 lists the pinout of connector BJ03.

Table 2.6: Connector BJ03

Pin Number	Signal	Pin Number	Signal
01	GND	02	GND
03		04	
05		06	
07		08	

Table 2.6: Connector BJ03 (Continued)

Pin Number	Signal	Pin Number	Signal
09		10	
11	SPBJ31/	12	SPBJ31
13	PERIN/	14	PERIN
15	INTIN/	16	INTIN
17	SPBJ30/	18	SPBJ30
19	DIN31/	20	DIN31
21	DIN30/	22	DIN30
23	DIN29/	24	DIN29
25	DIN28/	26	DIN28
27	DIN27/	28	DIN27
29	DIN26/	30	DIN26
31	DIN25/	32	DIN25
33	DIN24/	34	DIN24
35	DIN23/	36	DIN23
37	DIN22/	38	DIN22
39	DIN21/	40	DIN21
41	DIN20/	42	DIN20
43	DIN19/	44	DIN19
45	DIN18/	46	DIN18
47	DIN17/	48	DIN17
49	DIN16/	50	DIN16

Table 2.7 lists the pinout of connector BJ04.

Table 2.7: Connector BJ04

Pin Number	Signal	Pin Number	Signal
01	GND	02	GND
03	AOUT02	04	AOUT02/
05	AOUT03	06	AOUT03/
07	AOUT04	08	AOUT04/
09	AOUT05	10	AOUT05/

Table 2.7: Connector BJ04 (Continued)

Pin Number	Signal	Pin Number	Signal
11	AOUT06	12	AOUT06/
13	AOUT07	14	AOUT07/
15	AOUT08	16	AOUT08/
17	AOUT09	18	AOUT09/
19	AOUT10	20	AOUT10/
21	AOUT11	22	AOUT11/
23	AOUT12	24	AOUT12/
25	AOUT13	26	AOUT13/
27	AOUT14	28	AOUT14/
29	AOUT15	30	AOUT15/
31	BSYOUT	32	BSYOUT/
33	CLROUT	34	CLROUT/
35	WROUT	36	WROUT/
37	RDOUT	38	RDOUT/
39	CLKOUT	40	CLKOUT/
41	XECOUT	42	XECOUT/
43	HD2OUT	44	HD2OUT/
45	HD1OUT	46	HD1OUT/
47	DMAOUT	48	DMAOUT/
49	SCKOUT	50	SCKOUT/

Table 2.8 lists the pinout of connector BJ05.

Table 2.8: Connector BJ05

Pin Number	Signal	Pin Number	Signal
01	GND	02	GND
03		04	
05		06	
07		08	
09		10	
11	AOUT17/	12	AOUT17

Table 2.8: Connector BJ05 (Continued)

Pin Number	Signal	Pin Number	Signal
13	AOUT16/	14	AOUT16
15	ANSLOUT/	16	ANSLOUT
17	SPBJ50/	18	SPBJ50
19	DOUT15/	20	DOUT15
21	DOUT14/	22	DOUT14
23	DOUT13/	24	DOUT13
25	DOUT12/	26	DOUT12
27	DOUT11/	28	DOUT11
29	DOUT10/	30	DOUT10
31	DOUT09/	32	DOUT09
33	DOUT08/	34	DOUT08
35	DOUT07/	36	DOUT07
37	DOUT06/	38	DOUT06
39	DOUT05/	40	DOUT05
41	DOUT04/	42	DOUT04
43	DOUT03/	44	DOUT03
45	DOUT02/	46	DOUT02
47	DOUT01/	48	DOUT01
49	DOUT00/	50	DOUT00

Table 2.9 lists the pinout of connector BJ06.

Table 2.9: Connector BJ06

Pin Number	Signal	Pin Number	Signal
01	GND	02	GND
03		04	
05		06	
07		08	
09		10	
11	SPBJ61/	12	SPBJ61
13	PEROUT/	14	PEROUT

Table 2.9: Connector BJ06 (Continued)

Pin Number	Signal	Pin Number	Signal
15	OUTTOUT/	16	OUTTOUT
17	SPBJ60/	18	SPBJ60
19	DOUT31/	20	DOUT31
21	DOUT30/	22	DOUT30
23	DOUT29/	24	DOUT29
25	DOUT28/	26	DOUT28
27	DOUT27/	28	DOUT27
29	DOUT26/	30	DOUT26
31	DOUT25/	32	DOUT25
33	DOUT24/	34	DOUT24
35	DOUT23/	36	DOUT23
37	DOUT22/	38	DOUT22
39	DOUT21/	40	DOUT21
41	DOUT20/	42	DOUT20
43	DOUT19/	44	DOUT19
45	DOUT18/	46	DOUT18
47	DOUT17/	48	DOUT17
49	DOUT16/	50	DOUT16

Signal Definitions

Table 2.10 lists the functions of the signals that are delivered to the Digital Crate.

Table 2.10: Signal Descriptions, Digital Crate

Signal Name	Description
ADD[02-15]/	Address Bus.
DAT[00.31]/	Data Bus.
BUSCK/	Trillium Bus Clock.
ALL/	All pin write signal.
READ/	Read signal.
WRITE/	Write signal.

Table 2.10: Signal Descriptions, Digital Crate

Signal Name	Description
EXEC/	Execute signal.
SCLR/ *	System Clear signal.
BUSY/	Pattern Busy signal sent back to the TPAT2A from the digital control board (TSEQNT).
DMA/	Indicates DMA bus cycle.
INTOTMP/	Over temperature interrupt sent back to the CBIFNT and then the PWRBD.
HEAD01/	Test Head 1 select.
HEAD02/	Test Head 2 select.
INT0/	Interrupt 0 sent back to the CBIFNT.
INT1/	Interrupt 1 sent back to the CBIFNT.
INT2/	Interrupt 2 sent back to the CBIFNT.
INT3/	Interrupt 3 sent back to the CBIFNT.

* System clear (SCLR), is not directly associated with a particular bus cycle. This signal is generated by a write to a register on the TPAT2A.

Table 2.11 lists the functions of the signals that are delivered to the Analog Crate.

Table 2.11: Signal Descriptions, Analog Crate

Signal	Description
ADD[02-15]	Address Bus.
DAT[00.31]	Data Bus.
CLK	Trillium Bus Clock.
RD	Read signal.
WR	Write signal.
RST	System Clear signal.
HD1	Test Head 1 select.
HD2	Test Head 2 select.

Test Program Accelerator 2A (TPAT2A)

The Test Program Accelerator 2A (TPAT2A) is the interface board between the Tester Computing elements of an enVision controller and the test channels in the Fusion HF system. The TPAT2A communicates through the Trillium buses, G-link buses, and the VSB bus.

To control 1024 test channels, the TPAT2A supports four Trillium buses: Each Trillium bus supports up to 256 test channels (also known as tester pins). The "All Pin Write" function of the TPAT2A allows it to broadcast to all four Trillium Buses at the same time.

The primary functions of the TPAT2A are as follows:

- Digital Crate Interface, page 2-15
- Test Head Interface, page 2-16
- Accelerate pattern loads, page 2-17
- P I/O Controller, page 2-18

For information about the computing elements of the VME Crate, refer to the online manual.

Digital Crate Interface

To correctly deliver signals to the boards in the Digital Crate, the Bus Interface NT board (CBIFNT) re-synchronizes the Trillium bus control signals from the TPAT2A.

Figure 2.3 on page 2-16 shows the hardware interface from the enVision TPA CPU of the VME Crate to the boards in the Digital Crate.

For information about enVision, refer to the online manual.

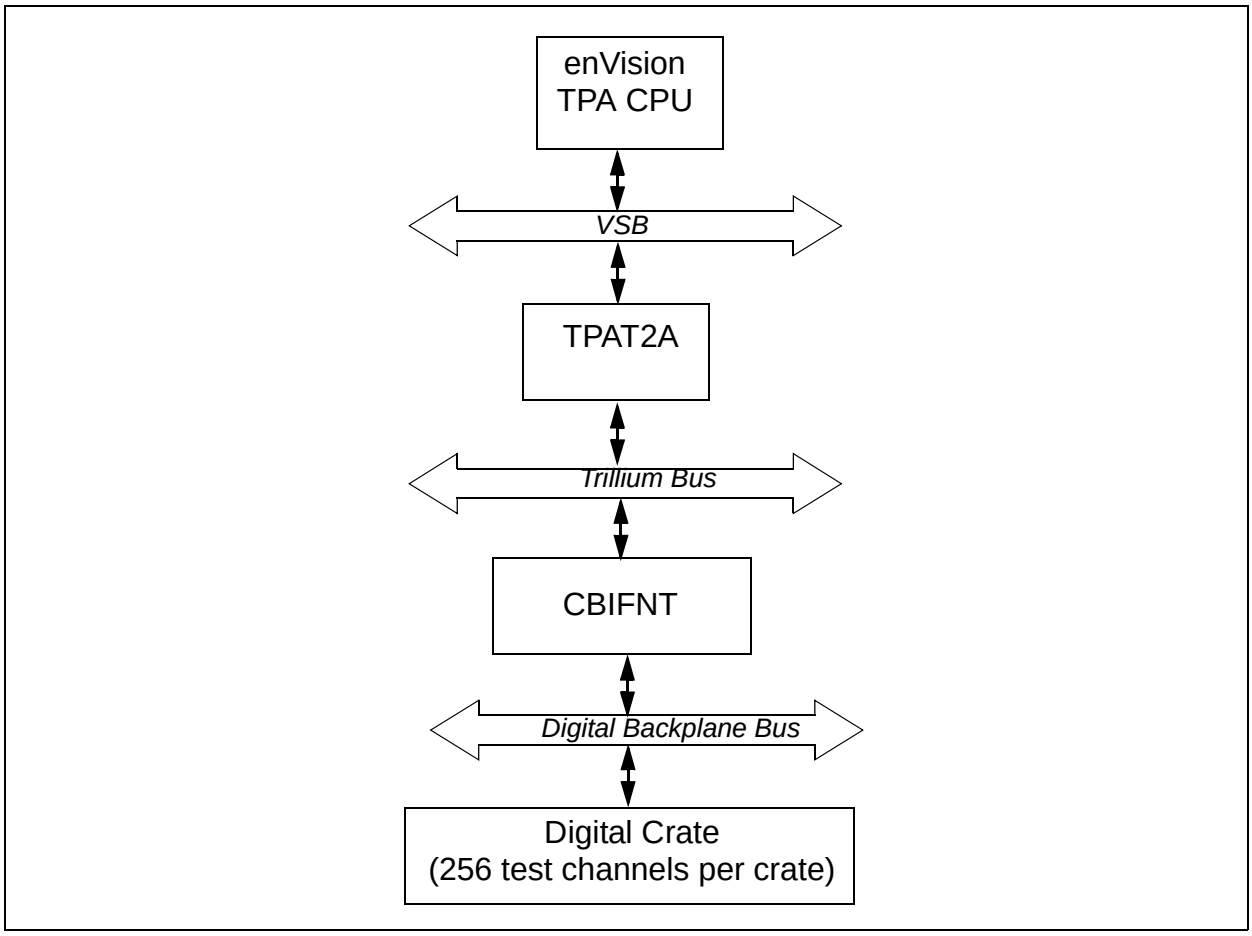


Figure 2.3: enVision Interface to Digital Crate

Test Head Interface

The test head interface is accomplished through the Turbo Load Board (TLBD) and the G-Link bus. As the G-Link chipset processes only 20-bit words per cycle, it uses four words to process the full functionality of the Trillium bus.

The G-Link bus, including the read/write interface, are described in G-Link Bus on page 2-24.

The TLBD board is described in Turbo Load Board (TLBD) on page 2-23.

Pattern Accelerator

The pattern accelerator caches blocks of pattern data from the Right-Local-Bus (RLB), then uses direct memory access (DMA) to deliver the pattern data to the tester.

Each block of pattern data can be written to as many as 16 tester channels. This supports testing multiple devices. The number of tester channels, as well as the pointers (addresses) to those channels are listed in a header in the block with the pattern data.

The pattern accelerator has four blocks of SRAM to cache up to four blocks of data from the RLB.

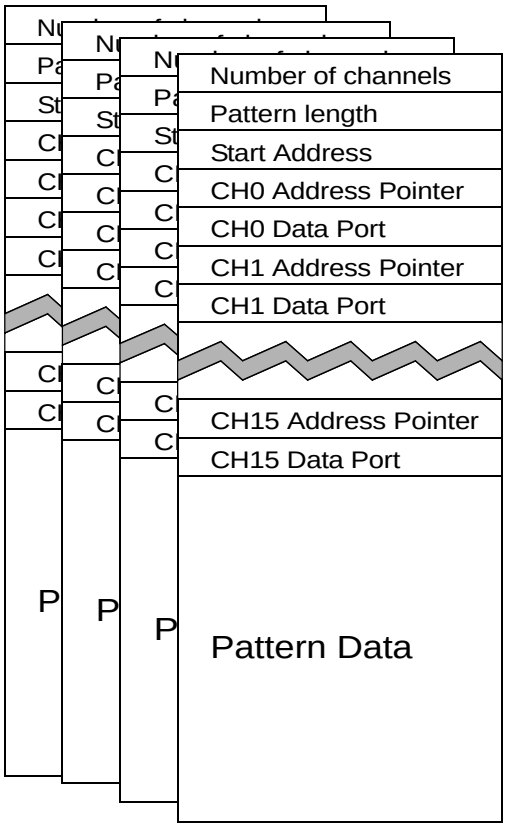
Data Blocks

TPAT2A accelerates pattern loads through a caching system. There are 4 blocks of SRAM, each of which can capture a 16k block of data. The data contains a prefix that describes how much data is in the block, where it needs to go, and the pattern data.

Each block of pattern data can be delivered to 1-16 test channels.

The first long-word in the pattern data block describes the number of tester channels that this pattern data will be written to. The second long-word is the number of 32-bit words in the pattern data block. The third long-word is the start address for the pattern in tester memory. The next block of long-words describe which test channels are associated with the pattern block.

Figure 2.4 shows the contents of pattern data blocks.



One TPAT2A board can support up to four Trillium buses; four data blocks are shown.

Figure 2.4: Test Pattern Data Blocks

P Input/Output Controller

The P Input/Output (P I/O) Controller allows the computing elements to communicate with the tester directly: the stored-state controller and the pattern accelerator are by-passed.

This controller is driven from the Right-Local-Bus (RLB), and drives the Left-Local-Bus (LLB).

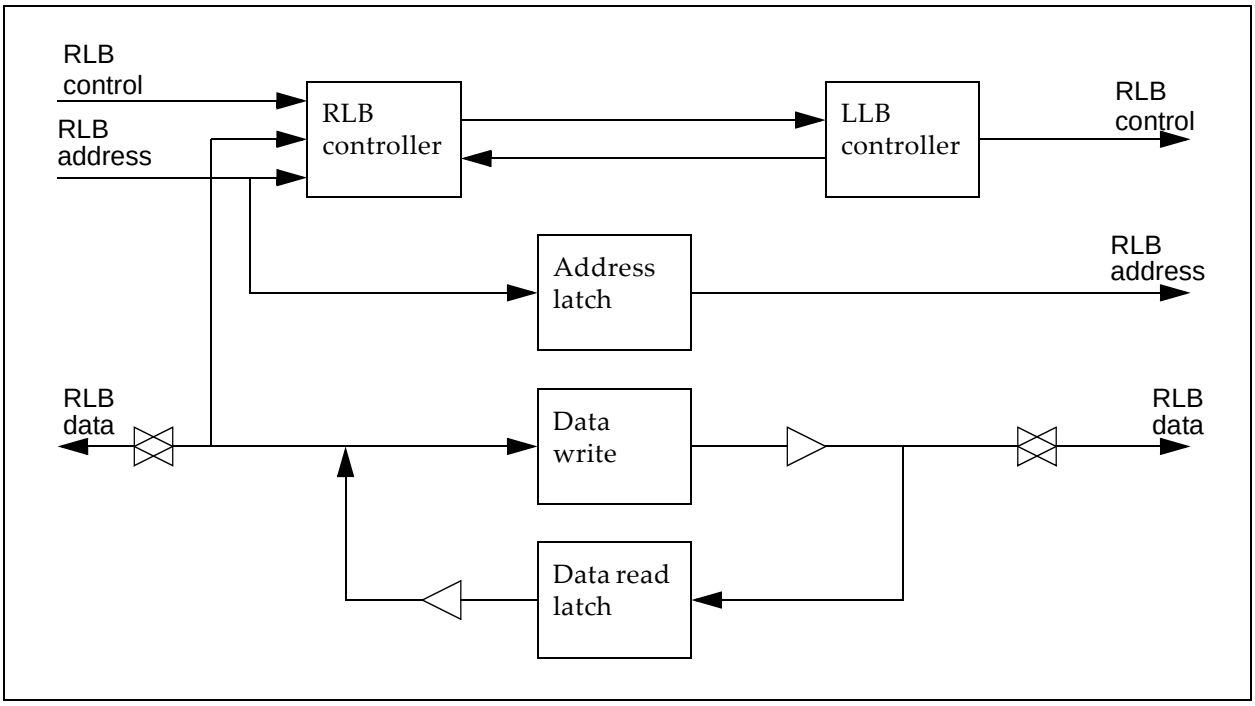


Figure 2.5: P I/O Block Diagram

Bus Interface

Figure 2.6 on page 2-20 shows a block diagram of the Fusion HF system bus architecture.

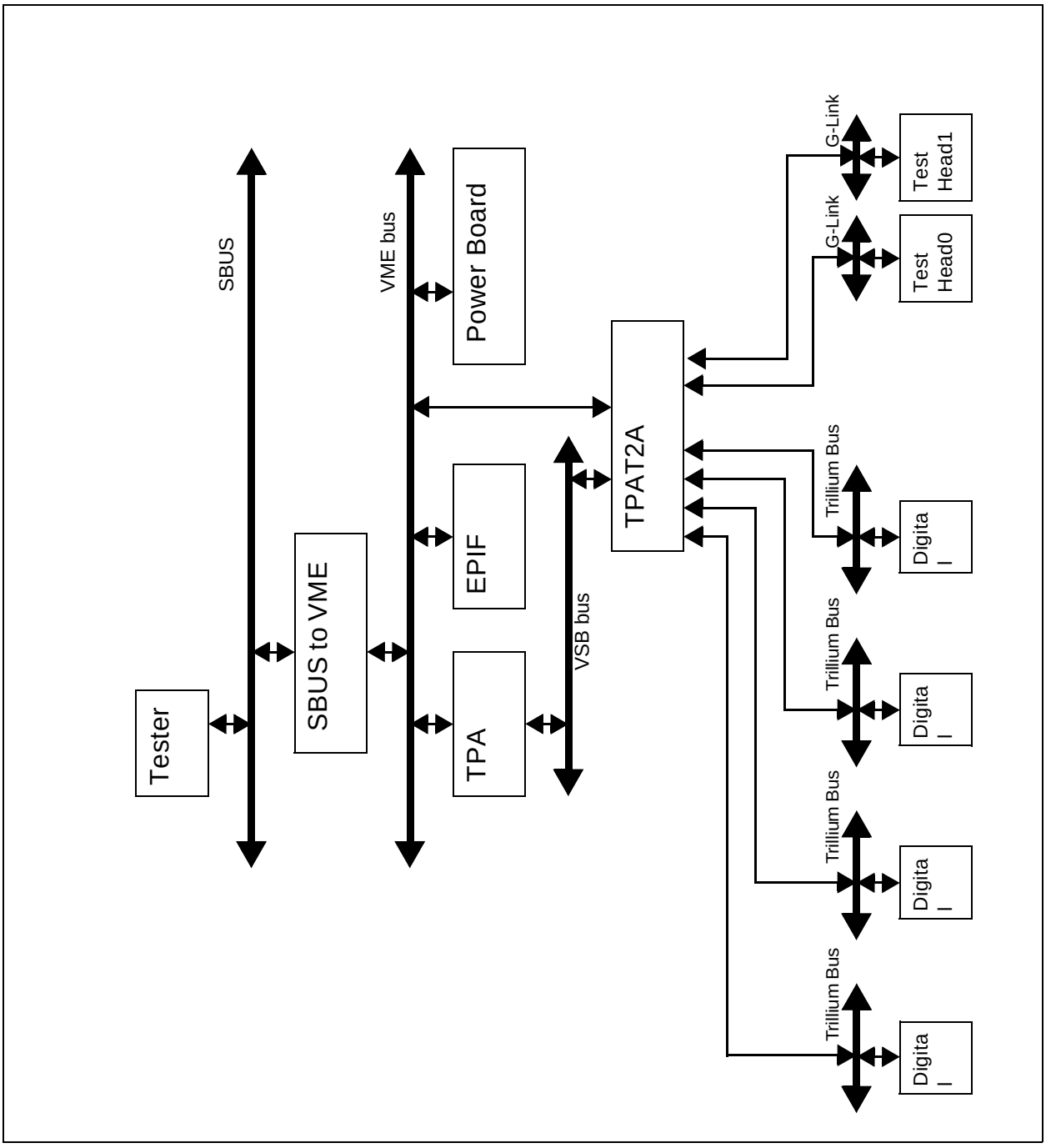


Figure 2.6: Fusion HF System Bus Architecture

Local Buses

The Right-Local-Bus (RLB) interfaces the VME bus and/or VSB controllers with the internal TPAT2A accelerator modules.

The Left-Local-Bus (LLB) interfaces the internal accelerators with the tester interfaces.

Table 2.12 lists the local bus signals.

Table 2.12: Local Bus Signals

Signal	Description
ADDR[27:0]	28 bit address bus, which is driven by the module currently holding the bus.
DATA[31:0]	32 bit data bus. In a write transaction, the data bus is driven by the module writing the data. In a read transaction, the data bus is driven by the module from which the data is to be read.
BR[6:0]*	7 bit request bus. One bit per device supported on the bus. Modules will pull on its bus request line if it needs to get on the bus.
BG[6:0]*	7 bit bus grant line. When the bus arbitrator gives permission for a module to get on the bus, it sets this line to logical low.
BUSY*	The bus is busy (in use). A module forces this signal when it is actively using the bus: This stops other modules from interrupting the bus activity.
WRITE*	This signal is be low when the transaction is *write* When the signal is high, the transaction is *read*.
AS*	This signal indicates that the address on the address bus is valid.
DACK*	In a write cycle, DACK* indicates that valid data has been latched into the slave. In a read cycle, DACK* indicates that valid data is on the data bus.
BUSCLR*	This signal tells all the modules to clear the bus.

Figure 2.7 shows the timing of a write cycle.

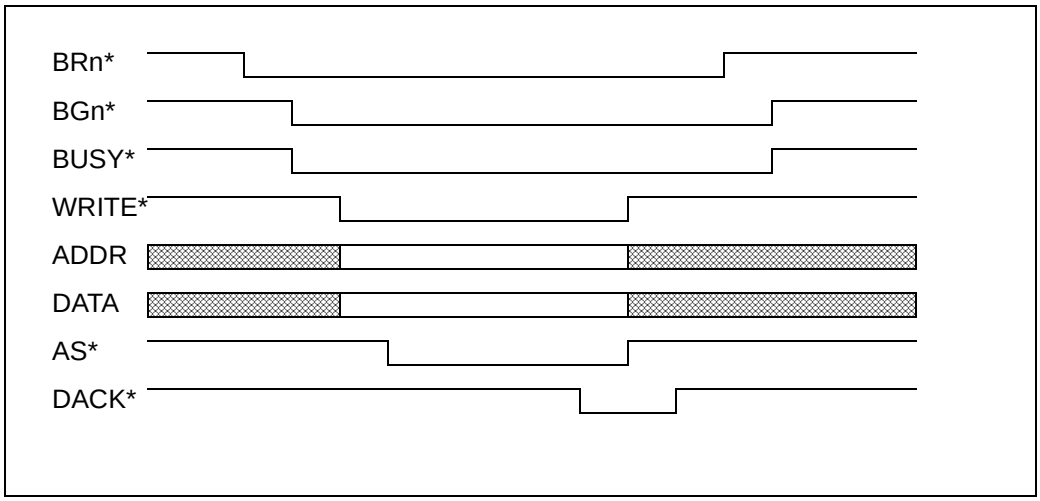


Figure 2.7: Local Bus Write Cycle

Figure 2.8 shows the timing of a read cycle.

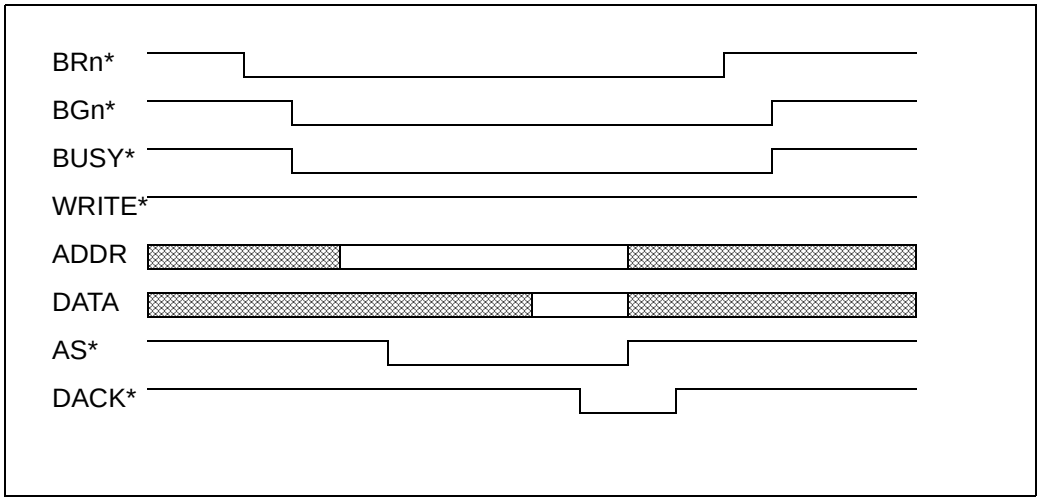


Figure 2.8: Local Bus Read Cycle

Bus Interface Connectors

The connectors for the cables on the TPAT2A are keyed by size and shape. Each Trillium bus is a differential ECL bus that is connected to the front panel of the TPAT2A through a set of two cables: a 50-pin cable, and a 100-pin cable.

Diagnostic Modes

Following are overviews of the two diagnostic modes available for the operation of pattern accelerator. For detailed information, refer to the online manual.

Diagnostic Mode 1

Mode 1 only tests the input cache memories. In this mode, the pattern accelerator allows readback of memory, but does not process the data.

Diagnostic Mode 2

Mode 2 tests the pattern buffer SRAM: a data block written to the input cache is ported to the pattern buffer SRAM, where it can be read back from the RLB. In this mode, the pattern accelerator does not perform direct memory access to the LLB.

Turbo Load Board (TLBD)

The Turbo Load Board (TLBD) interfaces the tester mainframe to the test head through the serial bus. To send data, parallel words are formatted to serial streams, then transmitted across the bus. Received serial data is formatted to parallel words, then distributed.

The functions of the TLBD include VSB interface, and VSB t0 G-Link bus interface. The TLBD board is located in the VME crate.

VSB Bus Interface

The TLBD communicates with the computing elements through the VSB interface as a slave. The TLBD is capable of 32-bit transactions through the VSB.

G-Link Trillium Bus

The TLBD communicates with the Fusion HF test head through the G-Link Bus. A maximum of 20 bits and be transferred per transaction; it requires four 20-bit words to communicate to the test head controller board.

Each G-Link bus can support 4096 test channels. However, the Fusion HF system is configured to support a maximum of 1024 test channels

G-Link Bus

The G-Link bus is a high speed serial bus that interfaces the Turbo Load Board (TLBD) and the Fusion HF test head. The G-Link bus is based on Hewlett Packard send and receive devices, HDMP-1022 and HDMP-1024. The hardware is at both ends of the G-Link bus.

The sending end of a G-Link bus transaction is often referred to as “host”; the receiving end is referred to as “slave”..

Figure 2.9 shows a block diagram of G-Link hardware.

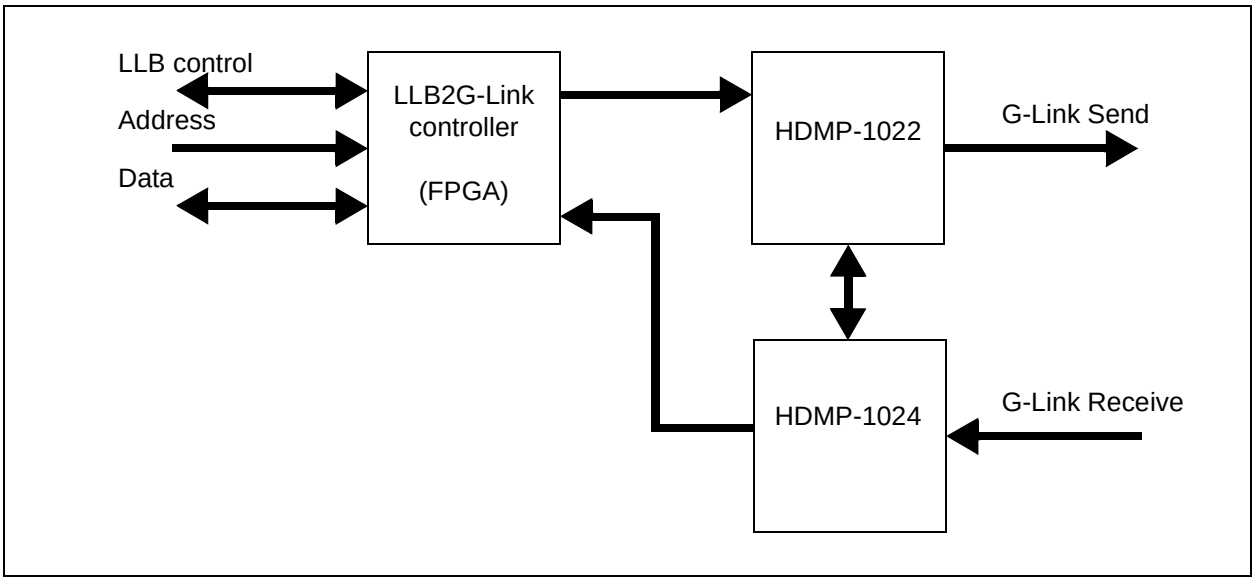


Figure 2.9: G-Link Block Diagram

NOTE This section outlines the basic G-Link functions. For detailed information, refer to the online manual, and to specifications provided by Hewlett Packard .

Serial Bus

The G-Link contains two unidirectional high speed serial bus paths: send, and receive. The data transfers contain the following: 24 bits for address; 32 bits for data; 16 bits for status information; 16 bits for fill frames.

Single Read/Write Transactions

Data is transferred in groups of frames. Figure 2.10 illustrates the read/write groups of data frames.

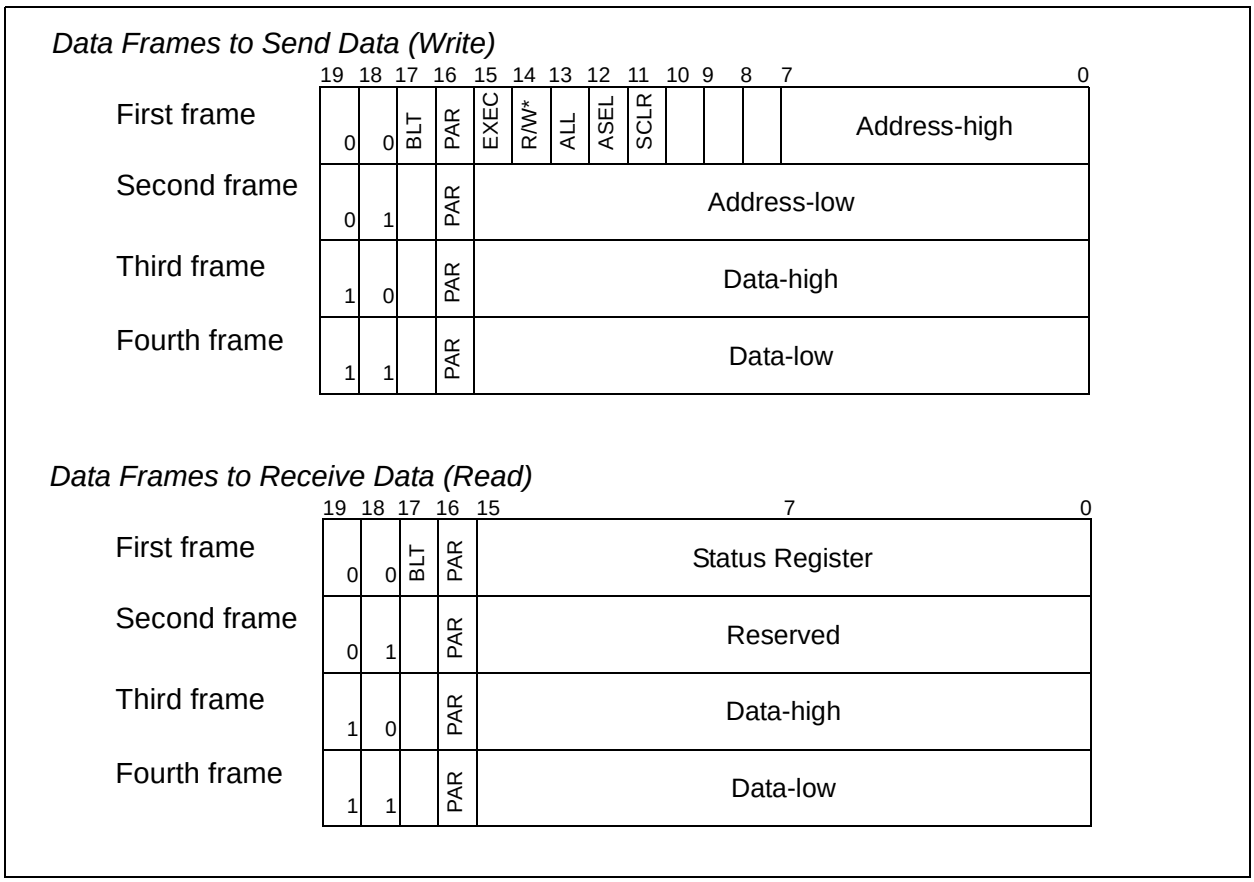


Figure 2.10: Read/Write Data Frames

Write Operation

Normal G-Link write transactions are single transactions that require four 20-bit frames.

- The test head interface controller reclocks (pipelines) the four 20-bit words, then echoes back the transaction to the G-Link controller. This informs the G-Link controller that the test head interface is ready for the next operation.

Read Operation

A read across the G-Link bus consists of two transactions.

- The write transaction delivers data frames across the send data bus to the test head interface controller. The first two frames supply the read address. The following two frames are ignored by the receiver. In all frames, the data fields are cleared.

- The TPAT2A then waits for the test head interface controller to respond with four 20-bit words. The requested data is delivered on the receive data bus.

Block Write Transaction

A block write allows an unlimited stream of data transfers: There is no limit to the amount of data that can be sent.

Bit 17 (BLT), when set to logical 1, indicates block transfer. Refer to Figure 2.10.

Status Frames and Fill Frames

During a transaction, 16 bits of status information is also transferred.

Filled frames only contain data to maintain the DC balance of the bus lines: filled data is not used.

Figure 2.11 shows the transfer of status information during single read/write transactions.

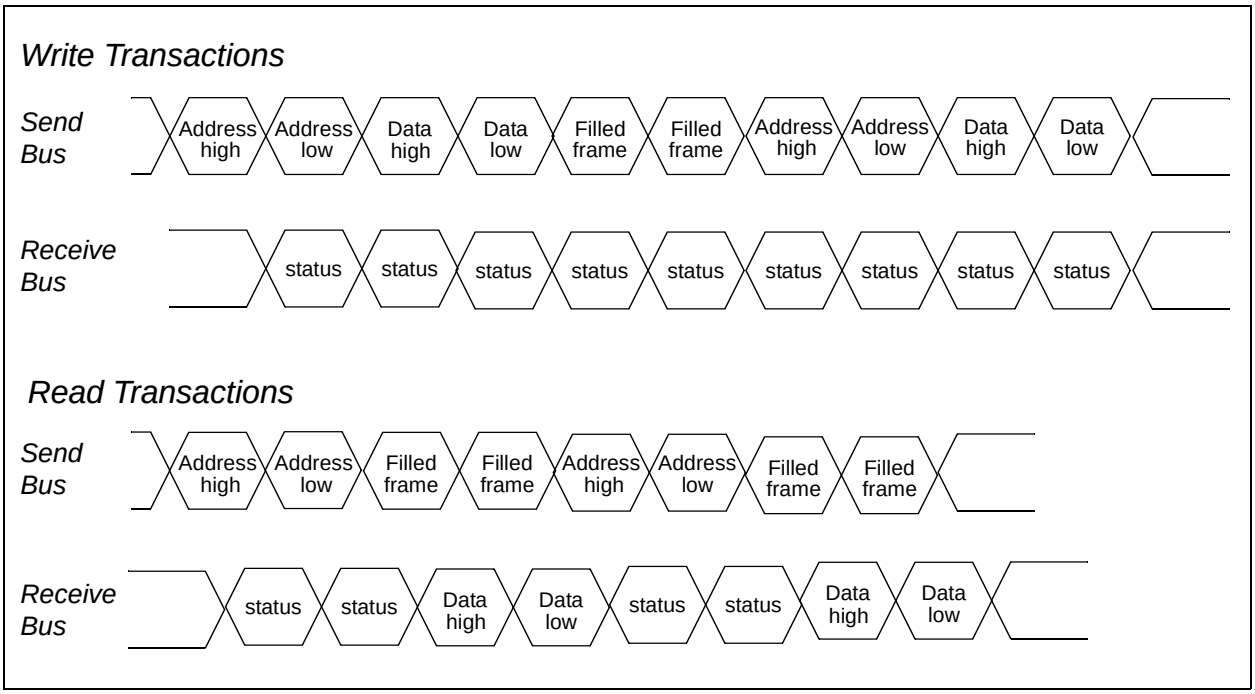


Figure 2.11: Status, Read/Write

Figure 2.12 shows the transfer of status information during block write transactions.

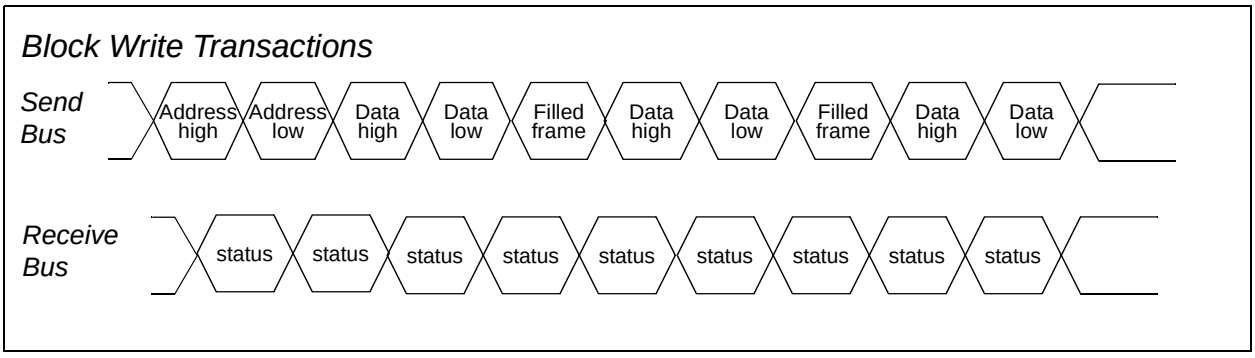


Figure 2.12: Status, Block Write

During block write transactions, filled frames are delivered if the receiving side of the G-Link bus is running slower.

Buffer Interface NT (CBIFNT)

The Buffer Interface NT (CBIFNT) printed circuit board provides the bus interface between the Digital Crate and the Test Program Accelerator (TPAT2A), and provides pass-through of the Trillium bus to other crates. One CBIFNT supports 256 test channels: There is one CBIFNT in each Digital Crate.

CBIFNT Functions

The primary functions of the CBIFNT board are:

- Information exchange with TPAT2A.
- Information exchange with other boards.
- Daisy chaining of buffered data, address and control signals to the other crates.
- Generate clock signals for each system board on the backplane.
- Wire-OR all the interrupts that are of the same type, then write to the status register of CBIFNT.
- Provide an Interrupt Mask/Test registe, to allow the masking of any interrupt signal — except “Thermal Interrupt,” and generate test interrupt signals.
- The “all pin write register” address is fully decoded, then generates the global signal ALLN to all system boards
- For diagnostics, allow the capture of any data or address that is used on the backplane bus. This is used as a read back test.

For more information on diagnostics, refer to the online manual.

Interface to TPAT2A

The CBIFNT re-synchronizes the Trillium bus control signals from the TPAT2A before passing them on to the other boards in the Digital Crate.

The CBIFNT interfaces to the TPAT2A through a 32-bit bi-directional data bus and a 16-bit address bus. Communication with TPAT2A and the next crate is through a differential ECL bus. Communication on the backplane is through a TTL bus.

- CBIFNT receives the following active low TTL signals: INT0N, INT1N, INT2N, INT3N, BUSYN, INTOTEMPN.
- CBIFNT generates the following active low TTL control signals: RDN, WRN, SCLRN, CLK0L-CLK3L, CLK0R-CLK3R, HD1N, HD2N, XECN, ALLN, HPARN, LPARN

Signal Pinout

Table 2.13 lists the pinout of the HDI connector, rows 1–3.

Table 2.13: CBINT HDI Connector Pinout, Rows 1–3

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1001	–5V	2001	–5V	3001	–5V
1002	ADD02*	2002	ADD03*	3002	ADD04*
1003	DGND	2003	DGND	3003	DGND
1004	ADD08*	2004	ADD09*	3004	ADD10*
1005	BUSCK*	2005	ADD14*	3005	ADD15*
1006	–	2006	–	3006	CLKSYNC
1007	DGND	2007	DGND	3007	DGND
1008	BUSY*	2008	TMPWR	3008	DMA*
1009	DAT00*	2009	DAT01*	3009	INT0*
1010	DAT02*	2010	DAT03*	3010	DAT04*
1011	DAT08*	2011	DAT09*	3011	DAT10*
1012	DGND	2012	DGND	3012	DGND
1013	DAT14*	2013	DAT15*	3013	DAT16*
1014	DAT20*	2014	DAT21*	3014	DAT22*
1015	DAT26*	2015	DAT27*	3015	DAT28*
1016	AIN02	2016	AIN02*	3016	–2V
1017	DGND	2017	DGND	3017	–
1018	AIN03	2018	AIN03*	3018	+15V

Table 2.13: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1019	AIN04	2019	AIN04*	3019	AIN05
1020	DGND	2020	DGND	3020	–15V
1021	AIN06	2021	AIN06*	3021	–
1022	AIN07	2022	AIN07*	3022	+5V
1023	DGND	2023	DGND	3023	AIN08
1024	AIN09	2024	AIN09*	3024	AIN10
1025	AIN11	2025	AIN11*	3025	–2V
1026	DGND	2026	DGND	3026	–2V
1027	AIN13	2027	AIN13*	3027	AIN12
1028	AIN14	2028	AIN14*	3028	DIN12*
1029	DGND	2029	DGND	3029	+3V
1030	BSYIN	2030	BSYIN*	3030	AIN15
1031	DGND	2031	DGND	3031	DIN09*
1032	CLRIN	2032	CLRIN*	3032	–2V
1033	WRIN	2033	WRIN*	3033	–2V
1034	DGND	2034	DGND	3034	RDIN
1035	CLKIN	2035	CLKIN*	3035	DIN06*
1036	XECIN	2036	XECIN*	3036	+3V
1037	DGND	2037	DGND	3037	HD2IN
1038	HD1IN	2038	HD1IN*	3038	DIN03*
1039	DMAIN	2039	DMAIN*	3039	–2V
1040	DGND	2040	DGND	3040	–2V
1041	SCKIN	2041	SCKIN*	3041	–
1042	–	2042	–	3042	–
1043	DGND	2043	DGND	3043	+5V
1044	–	2044	–	3044	–
1045	–2V	2045	–2V	3045	–2V
1046	–2V	2046	–2V	3046	–2V
1047	–	2047	–	3047	AOUT02

Table 2.13: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1048	DGND	2048	DGND	3048	–5V
1049	SPBJ31*	2049	SPBJ31	3049	–
1050	PERIN*	2050	PERIN	3050	AOUT05
1051	DGND	2051	DGND	3051	–2V
1052	INTIN*	2052	INTIN	3052	–2V
1053	SPBJ30*	2053	SPBJ30	3053	–2V
1054	DGND	2054	DGND	3054	AOUT09
1055	DIN31*	2055	DIN31	3055	+5V
1056	DIN29*	2056	DIN29	3056	DIN30*
1057	DGND	2057	DGND	3057	+3V
1058	DIN28*	2058	DIN28	3058	AOUT12
1059	DIN27*	2059	DIN27	3059	–2V
1060	DGND	2060	DGND	3060	–2V
1061	DIN26*	2061	DIN26	3061	–2V
1062	DGND	2062	DGND	3062	DIN25*
1063	DIN24*	2063	DIN24	3063	+3V
1064	DIN23*	2064	DIN23	3064	CLROUT
1065	DGND	2065	DGND	3065	+5V
1066	DIN22*	2066	DIN22	3066	–
1067	DIN21*	2067	DIN21	3067	–2V
1068	DGND	2068	DGND	3068	–2V
1069	DIN20*	2069	DIN20	3069	–2V
1070	DIN18*	2070	DIN18	3070	DIN19*
1071	DGND	2071	DGND	3071	HD1OUT
1072	DIN17*	2072	DIN17	3072	+5V
1073	DIN16*	2073	DIN16	3073	–
1074	DGND	2074	DGND	3074	–
1075	–	2075	–	3075	–2V
1076	DGND	2076	DGND	3076	–2V

Table 2.13: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1077	–	2077	–	3077	–2V
1078	–	2078	–	3078	–
1079	DGND	2079	DGND	3079	–
1080	–	2080	–	3080	+3V
1081	–	2081	–	3081	–
1082	DGND	2082	DGND	3082	–
1083	–	2083	–	3083	–2V
1084	SPBJ53*	2084	SPBJ53	3084	–2V
1085	DGND	2085	DGND	3085	–2V
1086	SPBJ52*	2086	SPBJ52	3086	–
1087	ANSELOUT*	2087	ANSELOUT	3087	INTOUT*
1088	DGND	2088	DGND	3088	–5V
1089	DOUT15*	2089	DOUT15	3089	SPBJ50*
1090	–2V	2090	–2V	3090	–2V
1091	–2V	2091	–2V	3091	–2V
1092	DOUT14*	2092	DOUT14	3092	DOUT30*
1093	DGND	2093	DGND	3093	+5V
1094	DOUT12*	2094	DOUT12	3094	DOUT13*
1095	DOUT11*	2095	DOUT11	3095	DOUT27*
1096	DGND	2096	DGND	3096	–2V
1097	DOUT10*	2097	DOUT10	3097	–2V
1098	DOUT08*	2098	DOUT08	3098	DOUT09*
1099	DGND	2099	DGND	3099	DOUT23*
1100	DOUT07*	2100	DOUT07	3100	+3V
1101	DOUT05*	2101	DOUT05	3101	DOUT06*
1102	DGND	2102	DGND	3102	DOUT20*
1103	DOUT04*	2103	DOUT04	3103	–2V
1104	DOUT03*	2104	DOUT03	3104	–2V
1105	DGND	2105	DGND	3105	DOUT02*

Table 2.13: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1106	DOUT01*	2106	DOUT01	3106	–
1107	DGND	2107	DGND	3107	+3V
1108	DOUT00*	2108	DOUT00	3108	–
1109	–	2109	–	3109	–
1110	DGND	2110	DGND	3110	–2V
1111	–	2111	–	3111	–2V
1112	–	2112	–	3112	–
1113	DGND	2113	DGND	3113	–
1114	–	2114	–	3114	+5V
1115	–	2115	–	3115	–
1116	DGND	2116	DGND	3116	–15V
1117	–	2117	–	3117	–
1118	–	2118	–	3118	+15V
1119	DGND	2119	DGND	3119	–
1120	–	2120	–	3120	–2V
1121	DGND	2121	DGND	3121	–2V
1122	–	2122	–	3122	–
1123	–	2123	–	3123	+3V
1124	DGND	2124	DGND	3124	–
1125	–	2125	–	3125	–
1126	–	2126	–	3126	–2V
1127	DGND	2127	DGND	3127	–2V
1128	–	2128	–	3128	–
1129	–	2129	–	3129	–
1130	DGND	2130	DGND	3130	+5V
1131	–	2131	–	3131	–
1132	–	2132	–	3132	–
1133	DGND	2133	DGND	3133	DGND
1134	INTOTMP*	2134	INTOREF	3134	–

Table 2.13: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1135	–5V	2135	–5V	3135	–5V

Table 2.14 lists the pinout of the HDI connector, rows 4–6.

Table 2.14: CBINT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4001	–5V	5001	–5V	6001	–5V
4002	ADD05*	5002	ADD06*	6002	ADD07*
4003	DGND	5003	DGND	6003	DGND
4004	ADD11*	5004	ADD12*	6004	ADD13*
4005	ALL*	5005	READ*	6005	WRITE*
4006	CLKSYNC*	5006	EXEC*	6006	SCLR*
4007	DGND	5007	DGND	6007	DGND
4008	INTOT*	5008	HEAD01*	6008	HEAD02*
4009	INT1*	5009	INT2*	6009	INT3*
4010	DAT05*	5010	DAT06*	6010	DAT07*
4011	DAT11*	5011	DAT12*	6011	DAT13*
4012	DGND	5012	DGND	6012	DGND
4013	DAT17*	5013	DAT18*	6013	DAT19*
4014	DAT23*	5014	DAT24*	6014	DAT25*
4015	DAT29*	5015	DAT30*	6015	DAT31*
4016	–2V	5016	–	6016	–
4017	–	5017	DGND	6017	DGND
4018	+15V	5018	SPBJ23*	6018	SPBJ23
4019	AIN05*	5019	SPBJ22*	6019	SPBJ22
4020	–15V	5020	DGND	6020	DGND
4021	–	5021	ANSELIN*	6021	ANSELIN
4022	+5V	5022	SPBJ20*	6022	SPBJ20
4023	AIN08*	5023	DGND	6023	DGND
4024	AIN10*	5024	DIN15*	6024	DIN15

Table 2.14: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4025	–2V	5025	DIN14*	6025	DIN14
4026	–2V	5026	DGND	6026	DGND
4027	AIN12*	5027	DIN13*	6027	DIN13
4028	DIN12	5028	DIN11*	6028	DIN11
4029	+3V	5029	DGND	6029	DGND
4030	AIN15*	5030	DIN10*	6030	DIN10
4031	DIN09	5031	DGND	6031	DGND
4032	–2V	5032	DIN08*	6032	DIN08
4033	–2V	5033	DIN07*	6033	DIN07
4034	RDIN*	5034	DGND	6034	DGND
4035	DIN06	5035	DIN05*	6035	DIN05
4036	+3V	5036	DIN04*	6036	DIN04
4037	HD2IN*	5037	DGND	6037	DGND
4038	DIN03	5038	DIN02*	6038	DIN02
4039	–2V	5039	DIN01*	6039	DIN01
4040	–2V	5040	DGND	6040	DGND
4041	–	5041	DIN00*	6041	DIN00
4042	–	5042	–	6042	–
4043	+5V	5043	DGND	6043	DGND
4044	–	5044	–	6044	–
4045	–2V	5045	–2V	6045	–2V
4046	–2V	5046	–2V	6046	–2V
4047	AOUT02*	5047	AOUT03	6047	AOUT03*
4048	–5V	5048	DGND	6048	DGND
4049	–	5049	AOUT04	6049	AOUT04*
4050	AOUT05*	5050	AOUT06	6050	AOUT06*
4051	–2V	5051	DGND	6051	DGND
4052	–2V	5052	AOUT07	6052	AOUT07*
4053	–2V	5053	AOUT08	6053	AOUT08*

Table 2.14: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4054	AOUT09*	5054	DGND	6054	DGND
4055	+5V	5055	AOUT10	6055	AOUT10*
4056	DIN30	5056	AOUT11	6056	AOUT11*
4057	+3V	5057	DGND	6057	DGND
4058	AOUT12*	5058	AOUT13	6058	AOUT13*
4059	–2V	5059	AOUT14	6059	AOUT14*
4060	–2V	5060	DGND	6060	DGND
4061	–2V	5061	AOUT15	6061	AOUT15*
4062	DIN25	5062	DGND	6062	DGND
4063	+3V	5063	BSYOUT	6063	BSYOUT*
4064	CLROUT*	5064	WROUT	6064	WROUT*
4065	+5V	5065	DGND	6065	DGND
4066	–	5066	RDOUT	6066	RDOUT*
4067	–2V	5067	CLKOUT	6067	CLKOUT*
4068	–2V	5068	DGND	6068	DGND
4069	–2V	5069	XECOUT	6069	XECOUT*
4070	DIN19	5070	HD2OUT	6070	HD2OUT*
4071	HD1OUT*	5071	DGND	6071	DGND
4072	+5V	5072	DMAOUT	6072	DMAOUT*
4073	–	5073	SCKOUT	6073	SCKOUT*
4074	–	5074	DGND	6074	DGND
4075	–2V	5075	–	6075	–
4076	–2V	5076	DGND	6076	DGND
4077	–2V	5077	–	6077	–
4078	–	5078	–	6078	–
4079	–	5079	DGND	6079	DGND
4080	+3V	5080	PSSYNC	6080	PSSYNC*
4081	–	5081	–	6081	–
4082	–	5082	DGND	6082	DGND

Table 2.14: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4083	–2V	5083	–	6083	–
4084	–2V	5084	SPBJ61*	6084	SPBJ61
4085	–2V	5085	DGND	6085	DGND
4086	–	5086	PEROUT*	6086	PEROUT
4087	INTOUT	5087	SPBJ60*	6087	SPBJ60
4088	–5V	5088	DGND	6088	DGND
4089	SPBJ50	5089	DOUT31*	6089	DOUT31
4090	–2V	5090	–2V	6090	–2V
4091	–2V	5091	–2V	6091	–2V
4092	DOUT30	5092	DOUT29*	6092	DOUT29
4093	+5V	5093	DGND	6093	DGND
4094	DOUT13	5094	DOUT28*	6094	DOUT28
4095	DOUT27	5095	DOUT26*	6095	DOUT26
4096	–2V	5096	DGND	6096	DGND
4097	–2V	5097	DOUT25*	6097	DOUT25
4098	DOUT09	5098	DOUT24*	6098	DOUT24
4099	DOUT23	5099	DGND	6099	DGND
4100	+3V	5100	DOUT22*	6100	DOUT22
4101	DOUT06	5101	DOUT21*	6101	DOUT21
4102	DOUT20	5102	DGND	6102	DGND
4103	–2V	5103	DOUT19*	6103	DOUT19
4104	–2V	5104	DOUT18*	6104	DOUT18
4105	DOUT02	5105	DGND	6105	DGND
4106	–	5106	DOUT17*	6106	DOUT17
4107	+3V	5107	DGND	6107	DGND
4108	–	5108	DOUT16*	6108	DOUT16
4109	–	5109	–	6109	–
4110	–2V	5110	DGND	6110	DGND
4111	–2V	5111	–	6111	–

Table 2.14: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4112	–	5112	–	6112	–
4113	–	5113	DGND	6113	DGND
4114	+5V	5114	–	6114	–
4115	–	5115	–	6115	–
4116	–15V	5116	DGND	6116	DGND
4117	–	5117	–	6117	–
4118	+15V	5118	–	6118	–
4119	–	5119	DGND	6119	DGND
4120	–2V	5120	–	6120	–
4121	–2V	5121	DGND	6121	DGND
4122	–	5122	–	6122	–
4123	+3V	5123	–	6123	–
4124	–	5124	DGND	6124	DGND
4125	–	5125	–	6125	–
4126	–2V	5126	–	6126	–
4127	–2V	5127	DGND	6127	DGND
4128	–	5128	–	6128	–
4129	–	5129	–	6129	–
4130	+5V	5130	DGND	6130	DGND
4131	–	5131	–	6131	–
4132	–	5132	–	6132	–
4133	DGND	5133	DGND	6133	DGND
4134	–	5134	–	6134	–
4135	–5V	5135	–5V	6135	–5V

Digital Crate 3

Introduction

In the Fusion HF test system, one Digital Crate supports 256 test channels. A maximum of four Digital Crates, 1024 test channels, can be installed in one HF tester.

- The Timing Control, Sequencer, Instruction Generator printed circuit board is the digital control board. The TSINT supports 256 test channels.
- The Buffer Interface NT (CBIFNT) board provides bus interface. The CBIFNT supports 256 test channels.
- The DW Buffer NT (DWBFNT) board provides interface between the TSINT and the other boards in the Digital Crate. One DWBFNT supports 128 test channels.
- One Format Response Memory NT (FARMNT) board delivers and receives test signals to and from the test head. One FARMNT supports 16 test channels.
- The Fail Log MemorY (FLMY) board is optional. It supports the test of memory devices. One FLMY supports 128 test channels.
- The Data Processor Response (DPRO) board is an optional. It supports the test of digital signal processors (DSP). One DPRO supports 128 test channels.
- There is one SPARE slot for future use.

The layout of the Digital Crate is shown in Figure 3.1 on page 3-2.

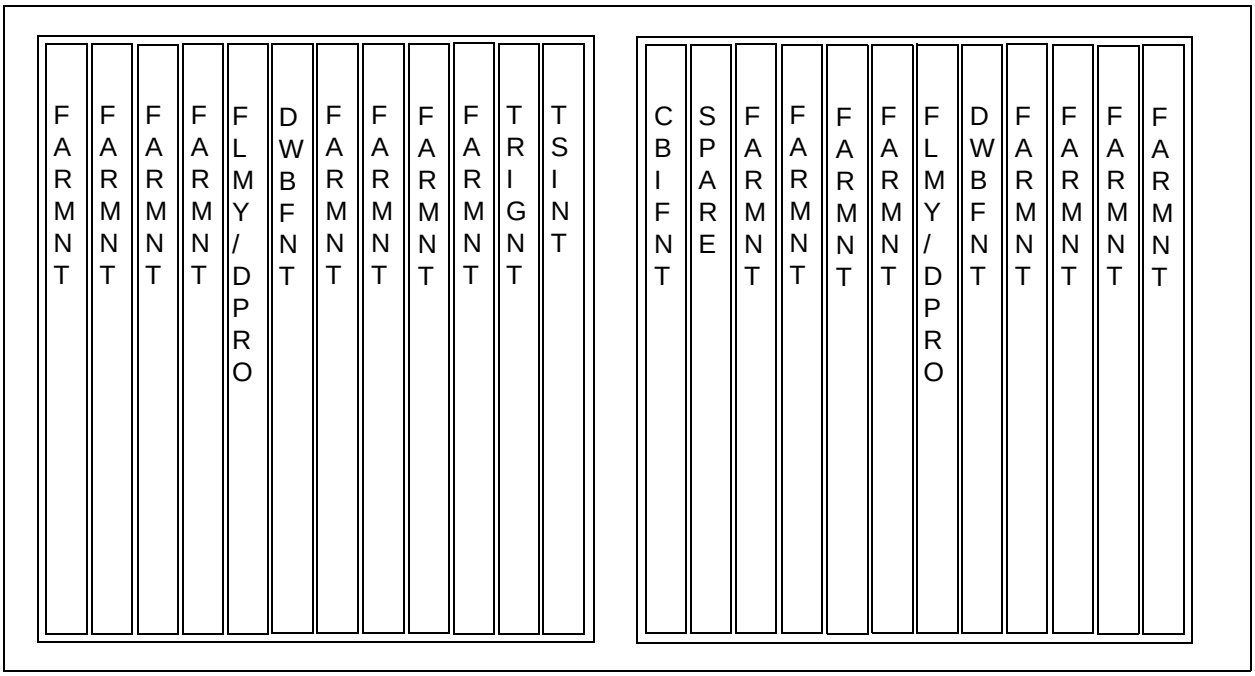


Figure 3.1: Digital Crate

Timing Control, Sequencer, Instruction Generator

The Timing Control, Sequencer and Instruction Generator NT (TSINT) board is the digital control board. It provides the period starts, controls the start up and shut down of test patterns, controls the sequencing, and generates CPM addresses and DPM start and repeat controls for the pattern subsystem. The TSINT board operates at rates up to 125 MHz.

One TSINT board supports 256 test channels. There is one TSINT board per Digital Crate. When more than one TSINT board is installed in the Fusion HF tester, one TSINT is the “master,” and the others are “slaves.” This is set up through the hardware configuration of the Digital Crate backplanes.

High Speed Data Interface

The TSINT interfaces signals within a Digital crate:

- All signals from the DWBFNT boards
- CTMU bus signals from the FARMNT boards

NOTE CTMU is an optional feature.

The following high speed signals that are delivered to the DWBFNT boards and the TRIGNT board:

- Period start clocks (CxxPS)
- System reference clock (31.25MHz)
- CPM address
- LTSA address
- DPM control signals

The following high speed signals are delivered to the FARMNT, FLMY, and DPRO boards:

- DPM start address

NOTE FLMY and DPRO are optional digital boards.

Reference Clock

TSINT provides the reference clock for the digital subsystem. The reference clock is 31.25MHz, which is generated from one of two sources: a crystal oscillator on the TSINT; the precision time source (PTS) input. The clock source is selected by the user. The default clock source is the PTS input.

All of the clocks in the pattern system are derived either directly or indirectly from this clock source. The reference clock also provides a reference signal for all phase locked loops (PLL) in the digital system.

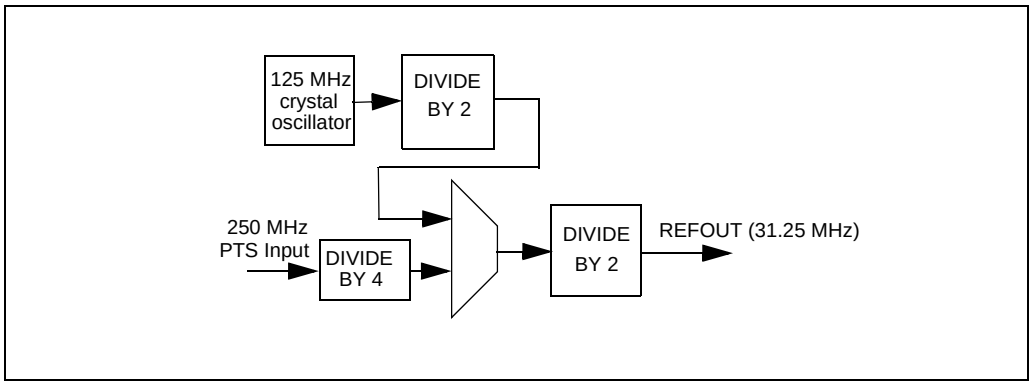


Figure 3.2: Reference Clock Source

Synchronize TSINT Boards

To synchronize multiple TSINTs in the system, four copies of the reference clock output are buffered from the master TSINT. One buffered copy of the clock is delivered to each of the slave TSINTs. The fourth copy is looped back to the master TSINT that supplies the clock.

All functions provided by this clock use the buffered versions of the clock.

Period Generator and Fail Signals

The period generator provides the digital system with period start clocks (CxxPS, also known as PS) for busy conditions and non-busy conditions.

When the system is non-busy the period generator produces 64ns periods with 8ns pulsewidth. When the system switches from non-busy to busy, the CxxPS pulsewidth changes from 8ns to 4ns.

A specific period start clock, C00PS, is used to generate the TSINT fail clock CFPS. CFPS clocks the fail enable signals and the ignore fail signals.

Instruction Generator and Sequencer

Figure 3.3 on page 3-7 shows a block diagram of the Instruction Generator, and the Sequencer functions.

Instruction Generator (IGEN)

The master TSINT ensures the Instruction Generator (IGEN) of each TSINT is synchronized.

CPM Instruction Memory

The CPM instruction read/write memory contains the CPM microinstructions, the CPM branch address, the CPM repeat count and the CPM mode bits.

This memory is accessed as two 16 bit memories, one vector per cycle. It supports autoincrement during both reading and writing of the memory.

CPM Instruction Generator

The CPM instruction generator controls the CPM address based on the contents of the CPM instruction memory. TSINT distributes copies of the CPM address, enable and clock information to the two DWBFNT boards in the Digital Crate.

This instruction generator supports the following microinstructions:

Table 3.1: CPM Instructions

Instruction	Description
COND	Select condition for conditional operations
JSR	Unconditional jump to a subroutine address
CJSR	Conditional jump to a subroutine address
JMP	Unconditional jump to a new address
CJMP	Conditional jump to a new address
RET	Unconditional return from a subroutine
CRET	Conditional return from a subroutine
JSRI	Unconditional jump to a subroutine using the indirect address
CJSRI	Conditional jump to a subroutine using the indirect address
RPT	Repeat the current CPM address
RPTP	Repeat the current address until the DUT passes
FLAG	Set or clear one or more flag bits
MODE	fsSet or clear one or more mode bits

Table 3.1: CPM Instructions (Continued)

Instruction	Description
LCR1	Load counter 1 with a value
LCR2	Load counter 2 with a value
LCR3	Load counter 3 with a value
LCR4	Load counter 4 with a value
DC1	Decrement counter 1
DC2	Decrement counter 2
DC3	Decrement counter 3
DC4	Decrement counter 4

DPM Instruction Generator

The DPM instruction generator controls the DPM address. This address is not distributed to other boards in the system, however the control signals used to generate the address are distributed to the DWBFNT boards, and the start address is delivered to the FARMNT boards.

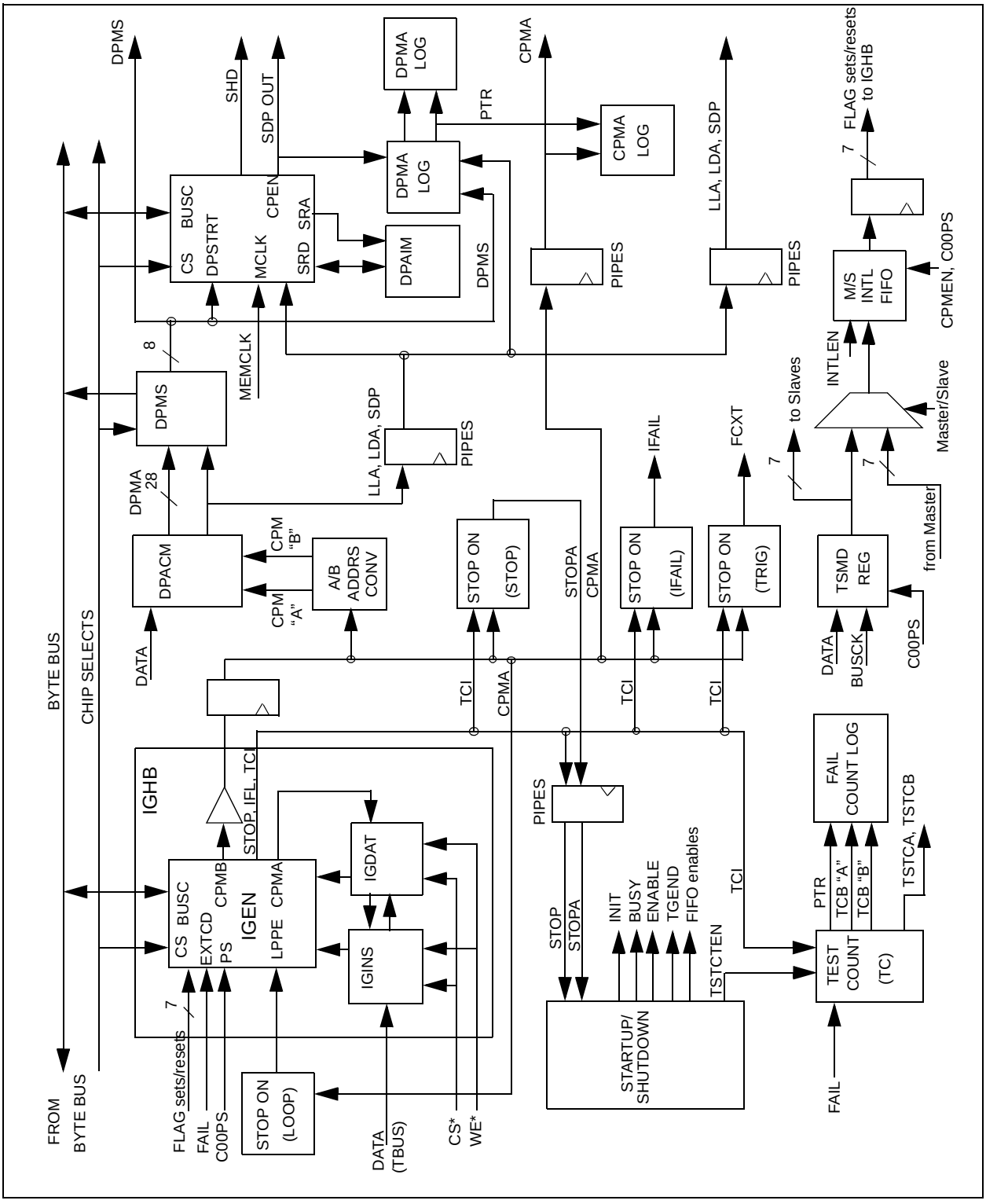


Figure 3.3: Instructor Generator and Sequencer

Sequencer Control Logic

The sequence control logic controls the test pattern start up, and the test pattern shut down.

The Stop, Stop Fail, Ignore Fail, and Test Count Inhibit signals are generated by CPM instructions.

Stop Test Patterns

There are three modes to stop test patterns:

- Stop On Address
- Stop On Count
- Stop On Address and Count

Stop On Address. Stop on address is provided by comparing a stored stop address with the CPMA on each cycle. When they match, a stop signal is sent to the sequence control logic.

Stop On Count. Stop on count is provided by a test counter that counts down from the stored stop value. When the counter reaches zero the stop signal is sent to the sequence control logic. The stop counter is reloaded by INIT at the start of each pattern execution.

The counter normally does not count when the test count inhibit (TCI) signal is true. However, there is a mode bit that will allow it to count when TCI is true.

Stop On Address Plus Count. In this mode, when the address compare is true, the stop on count test counter is started instead of sending the stop signal to the sequence control logic. The pattern then stops normally when the test counter.

The stop on address plus count mode is provided by combining stop on address mode with the stop on count mode.

Fail Log

The TSINT has four types of fail logs:

- One fail status register
- Two log memories: Fail Count Log; Fail Quad Log

- Fail Counter

Fail Status Register

The Fail Status Register logs the fail bit pairs for each 64 test channel group, and the fail bit pairs from each FLMY/DPRO of the Fusion HF tester. When one of these bits is set, it remains set for the remainder of the pattern execution. These bits are cleared to “0” at the start of pattern execution by the INIT signal.

All low speed ignore fail modes except the global ignore fail prevent logging of fails to this register. This register also logs fails from the slave TSINTs.

Log Memory

The two log memories are Fail Count Log and Fail Quad Log.

Fail Count Log. When a device under test (DUT) fail occurs, the memories are written and the pointer is incremented. Through the address of the pointer, this log contains the test count (uninhibited and inhibited) at which a fail has occurred.

Fail log identifies the failing test cycles. In normal mode the fail count log wraps around after 1K locations. In fails only mode it stops logging after 1K locations.

The ignore fail signal can be inhibited from affecting the fail count: The Fail Count log does not log counts when the high speed ignore fail signal is true.

The Fail Count Log consists of two memories: memory A and memory B.

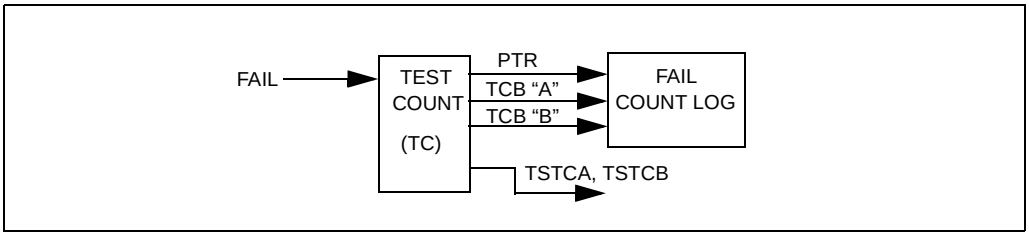


Figure 3.4: Fail Count Log

Fail Quad Log. The Fail Quad Log is part of the CPM address log memory. It stores data at half rate on alternating odd/even cycles. The A memory is read for even cycles and the B memory for odd cycles.

It logs two fail bits from each 128 test channel segment (group of 8 FARMNT boards), and can store two fail bits from each FLMY (optional Digital Crate board).

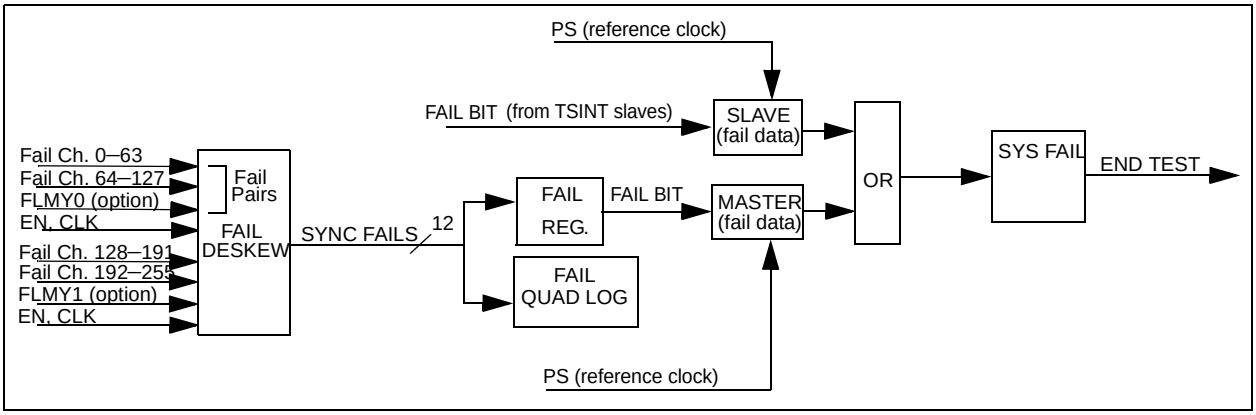


Figure 3.5: Fail Log

Fail Counter

The Fail Counter counts down the number fails: The counter begins at the number of the maximum allowed fails, then counts down towards zero. When the counter reaches zero, the delivery of the test pattern to the DUT is stopped. t

The Fail Counter is illustrated in Figure 3.4 on page 3-9

Fail Mask

The purpose of fail masking is to ignore selected DUT failures. There are two kinds of fail masking used on the TSINT: low speed and high speed fail masking.

Low Speed Fail Mask

The low speed mask can be set to mask selected individual bits, or to mask globally.

Individual Mask. The individual mask bits block the individual 128 test channel fail pairs from reaching any of the fail logging, matching or branching logic on the master TSINT, and from reaching the slave TSINTs in a tester configured with multiple Digital Crates.

There are two fail masks, one for each group of FARMNT boards.

Global Mask. The global fail mask prevents the following when a DUT fail occurs:

- Stop pattern execution
- Branching
- Log fail count
- Deliver fail data to the slave TSINTs

The global fail mask does allow fails to be logged in the fail status register.

High Speed Fail Mask

The high speed fail masking is provided by two sources: a CPM instruction. The ignore fail by count and or address logic on the TSINT.

The high speed fail masking prevents the following when a DUT fail occurs:

- Stop pattern execution
- Log fail count

The high speed fail mask does not block fails to the slave TSINTs, or the branch on fail capability on the master TSINT.

Log Fails Only

In Log Fails Only mode, the address logs for CPMA, DPMA, and LTSA, the Period Accumulate Log and the Fail Quad log only record data when a fail is detected; not all DUT response is recorded.

When a fail is detected, the log memories are written and their pointers are incremented.

Ignore Fail

Specified fails can be ignored: not recorded. There are three modes of Ignore Fail:

- Ignore fail on address
- Ignore fail on count
- Ignore fail on address plus count.
- Ignore fail instruction from IGEN.

Ignore Fail on Address. The controlled pattern memory address (CPMA) provides the address to ignore if a failure occurs. The CPMA provides an address each test cycle.

Ignore Fail on Count. A test counter tracks the number of test cycles to ignore DUT failures if they occur.

Ignore Fail on Address plus Count. The ignore fail on address and count mode combines the ignore fail on address mode with the ignore fail on count mode. The specified number of failures that occur at the selected test addresses are ignored.

Sequential Match

The Sequential Match mode determines if the test program vectors match the expected response from the DUT. Any number of passing vectors may be matched and a programmable set of passing/failing vectors may also be matched.

A programmable shift register on the TSINT keeps track of the DUT passes and fails.

Signal I/O

Table 3.2 shows the signal pinout for rows 1 - 3 of the high density interface (HDI) connectors. The section System Interface on page 3-22 describes the functions of the signals.

Table 3.2: TSINT HDI Connector Pinout, Rows 1–3

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1001	–5V	2001	–5V	3001	–5V

Table 3.2: TSINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1002	ADD02*	2002	ADD03*	3002	ADD04*
1003	DGND	2003	DGND	3003	DGND
1004	ADD08*	2004	ADD09*	3004	ADD10*
1005	BUSCK*	2005	ADD14*	3005	ADD15*
1006	SLAVE	2006	–	3006	CLKSYNC
1007	DGND	2007	DGND	3007	DGND
1008	BUSY*	2008	TMPWR	3008	DMA*
1009	DAT00*	2009	DAT01*	3009	INT0*
1010	DAT02*	2010	DAT03*	3010	DAT04*
1011	DAT08*	2011	DAT09*	3011	DAT10*
1012	DGND	2012	DGND	3012	DGND
1013	DAT14*	2013	DAT15*	3013	DAT16*
1014	DAT20*	2014	DAT21*	3014	DAT22*
1015	DAT26*	2015	DAT27*	3015	DAT28*
1016	CLOUT0	2016	CLOUT0*	3016	–2V
1017	DGND	2017	DGND	3017	OUTEN0
1018	FSYS0	2018	FSYS0*	3018	+15V
1019	CONT0	2019	CONT0*	3019	FSYS1
1020	DGND	2020	DGND	3020	–15V
1021	FL1S0	2021	FL1S0*	3021	FL1R0
1022	FL2S0	2022	FL2S0*	3022	+5V
1023	DGND	2023	DGND	3023	FL2S1
1024	FL2R0	2024	FL2R0*	3024	FL3S0
1025	FL3R0	2025	FL3R0*	3025	–2V
1026	DGND	2026	DGND	3036	–2V
1027	FL4S0	2027	FL4S0*	3027	FL3R1
1028	FL4R0	2028	FL4R0*	3028	STRT0
1029	DGND	2029	DGND	3029	+3V
1030	FBAY0	2030	FBAY0*	3030	STRT1

Table 3.2: TSINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1031	DGND	2031	DGND	3031	INEN0
1032	CLIN0	2032	CLIN0*	3032	–2V
1033	CLOUT2	2033	CLOUT2*	3033	–2V
1034	DGND	2034	DGND	3034	CLINS
1035	OUTEN2	2035	OUTEN2*	3035	FSYS2
1036	CONT2	2036	CONT2*	3036	+3V
1037	DGND	2037	DGND	3037	CONTS
1038	FL1S2	2038	FL1S2*	3038	FL1R2
1039	FL2S2	2039	FL2S2*	3039	–2V
1040	DGND	2040	DGND	3040	–2V
1041	FL2R2	2041	FL2R2*	3041	FL2SS
1042	FL3S2	2042	FL3S2*	3042	FL3R2
1043	DGND	2043	DGND	3043	–5V
1044	FL4S2	2044	FL4S2*	3044	FL3RS
1045	–2V	2045	–2V	3045	–2V
1046	–2V	2046	–2V	3046	–2V
1047	FL4R2	2047	FL4R2*	3047	STRT2
1048	DGND	2048	DGND	3048	–5V
1049	FBAY2	2049	FBAY2*	3049	STRTS
1050	INEN2	2050	INEN2*	3050	CLIN2
1051	DGND	2051	DGND	3051	–2V
1052	ACCLK0	2052	ACCLK0*	3052	–2V
1053	ACCLK1	2053	ACCLK1*	3053	–2V
1054	DGND	2054	DGND	3054	RFCLKM
1055	SCSYNC0	2055	SCSYNC0*	3055	+5V
1056	LTSA0M	2056	LTSA1M	3056	ACTRIG
1057	DGND	2057	DGND	3057	+3V
1058	FAILPSL	2058	FAILPSL*	3058	LTSA4M
1059	FAILENL	2059	IFAILL	3059	–2V

Table 3.2: TSINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1060	DGND	2060	DGND	3060	–2V
1061	FAIL0LL	2061	FAIL0UL	3061	–2V
1062	DGND	2062	DGND	3062	PTSIN
1063	FAIL1LL	2063	FAIL1UL	3063	+3V
1064	TGENM	2064	EPENM	3064	EVFLAG
1065	DGND	2065	DGND	3065	+5V
1066	WTRIGM	2066	INITM	3066	PBSYM
1067	DPMLDAM	2067	DPMLLAM	3067	–2V
1068	DGND	2068	DGND	3068	–2V
1069	REFCLKL	2069	REFCLKL*	3069	–2V
1070	REFCLKR	2070	REFCLKR*	3070	CPMA02M
1071	DGND	2071	DGND	3071	CPMA06M
1072	REFOUT0	2072	REFOUT0*	3072	+5V
1073	REFOUT2	2073	REFOUT2*	3073	CPMA08M
1074	DGND	2074	DGND	3074	CPMA10M
1075	DCOMPL	2075	DCOMPL*	3075	–2V
1076	DGND	2076	DGND	3076	–2V
1077	DCIN0	2077	DCIN0*	3077	–2V
1078	DCIN2	2078	DCIN2*	3078	CPMA12M
1079	DGND	2079	DGND	3079	CPMA14M
1080	DPSTRIG	2080	DPSTRIG*	3080	+3V
1081	CFPSL	2081	CFPSL*	3081	PTSTH1
1082	DGND	2082	DGND	3082	PTSTH2
1083	C00PSL	2083	C00PSL*	3083	–2V
1084	LTSA0L	2084	LTSA1L	3084	–2V
1085	DGND	2085	DGND	3085	–2V
1086	LTSA2L	2086	LTSA3L	3086	LTSA4L
1087	LTSA5L	2087	FFENL	3087	FFDENL

Table 3.2: TSINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1088	DGND	2088	DGND	3088	–5V
1089	FFLENL	2089	TGENL	3089	EPENL
1090	–2V	2090	–2V	3090	–2V
1091	–2V	2091	–2V	3091	–2V
1092	WTRIGL	2092	INITL	3092	REFIN
1093	DGND	2093	DGND	3093	+5V
1094	PBSYL	2094	DPMSDPL	3094	DCOUT
1095	DPMSHDL	2095	DPMLDAL	3095	DPMLLAL
1096	DGND	2096	DGND	3096	–2V
1097	CPMAENL	2097	CPMA00L	3097	–2V
1098	CPMA01L	2098	CPMA02L	3098	CPMA03L
1099	DGND	2099	DGND	3099	CPMA04L
1100	CPMA05L	2100	CPMA06L	3100	+3V
1101	CPMA07L	2101	CPMA08L	3101	CPMA09L
1102	DGND	2102	DGND	3102	CPMA10L
1103	CPMA11L	2103	CPMA12L	3103	–2V
1104	CPMA13L	2104	CPMA14L	3104	–2V
1105	DGND	2105	DGND	3105	CPMA15L
1106	DPMSPSAL	2106	DPMSLAAL	3106	DPMSPSBL
1107	DGND	2107	DGND	3107	+3V
1108	DPMS0AL	2108	DPMSLABL	3108	DPMS0BL
1109	DPMS1AL	2109	DPMS2AL	3109	DPMS1BL
1110	DGND	2110	DGND	3110	–2V
1111	DPMS3AL	2111	DPMS2BL	3111	–2V
1112	DPMS4AL	2112	DPMS5AL	3112	DPMS3BL
1113	DGND	2113	DGND	3113	DPMS4BL
1114	DPMS6AL	2114	DPMS5BL	3114	+5V
1115	DPMS7AL	2115	DPMS6BL	3115	DPMS7BL

Table 3.2: TSINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1116	DGND	2116	DGND	3116	–15V
1117	ACP0AL	2117	ACP0AL*	3117	PTSAIN
1118	ACP1AL	2118	ACP1AL*	3118	+15V
1119	DGND	2119	DGND	3119	ACP1M
1120	ACP0BL	2120	ACP0BL*	3120	–2V
1121	DGND	2121	DGND	3121	–2V
1122	ACP1BL	2122	ACP1BL*	3122	ACP0CL
1123	ACP0DL	2123	ACP0DL*	3123	+3V
1124	DGND	2124	DGND	3124	ACP1CL
1125	ACP1DL	2125	ACP1DL*	3125	ACP0DR
1126	ACP0EL	2126	ACP0EL*	3126	–2V
1127	DGND	2127	DGND	3127	–2V
1128	ACP1EL	2128	ACP1EL*	3128	ACP1DR
1129	ACP0FL	2129	ACP0FL*	3129	ACP1FL
1130	DGND	2130	DGND	3130	+5V
1131	ACP0GL	2131	ACP0GL*	3131	ACP1GL
1132	ACP0HL	2132	ACP0HL*	3132	ACP0GR
1133	DGND	2133	DGND	3133	DGND
1134	ACP1HL	2134	ACP1HL*	3134	ACP0HR
1135	–5V	2135	–5V	3135	–5V

Table 3.3 shows the signal pinout for rows 4 - 6 of the HDI connector. The section System Interface on page 3-22 describes the functions of the signals.

Table 3.3: TSINT HDI Connector Pinout, Rows 4 – 6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4001	–5V	5001	–5V	6001	–5V
4002	ADD05*	5002	ADD06*	6002	ADD07*
4003	DGND	5003	DGND	6003	DGND

Table 3.3: TSINT HDI Connector Pinout, Rows 4 – 6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4004	ADD11*	5004	ADD12*	6004	ADD13*
4005	ALL*	5005	READ*	6005	WRITE*
4006	CLKSYNC*	5006	EXEC*	6006	SCLR*
4007	DGND	5007	DGND	6007	DGND
4008	INTOT*	5008	HEAD01*	6008	HEAD02*
4009	INT1*	5009	INT2*	6009	INT3*
4010	DAT05*	5010	DAT06*	6010	DAT07*
4011	DAT11*	5011	DAT12*	6011	DAT13*
4012	DGND	5012	DGND	6012	DGND
4013	DAT17*	5013	DAT18*	6013	DAT19*
4014	DAT23*	5014	DAT24*	6014	DAT25*
4015	DAT29*	5015	DAT30*	6015	DAT31*
4016	–2V	5016	CLOUT1	6016	CLOUT1*
4017	OUTEN0*	5017	DGND	6017	DGND
4018	+15V	5018	OUTEN1	6018	OUTEN1*
4019	FSYS1*	5019	CONT1	6019	CONT1*
4020	–15V	5020	DGND	6020	DGND
4021	FL1R0*	5021	FL1S1	6021	FL1S1*
4022	+5V	5022	FL1R1	6022	FL1R1*
4023	FL2S1*	5023	DGND	6023	DGND
4024	FL3S0*	5024	FL2R1	6024	FL2R1*
4025	–2V	5025	FL3S1	6025	FL3S1*
4026	–2V	5026	DGND	6026	DGND
4027	FL3R1*	5027	FL4S1	6027	FL4S1*
4028	STRT0*	5028	FL4R1	6028	FL4R1*
4029	+3V	5029	DGND	6029	DGND
4030	STRT1*	5030	FBAY1	6030	FBAY1*
4031	INEN0*	5031	DGND	6031	DGND
4032	–2V	5032	INEN1	6032	INEN1*

Table 3.3: TSINT HDI Connector Pinout, Rows 4 – 6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4033	–2V	5033	CLIN1	6033	CLIN1*
4034	CLINS*	5034	DGND	6034	DGND
4035	FSYS2*	5035	INENS	6035	INENS*
4036	+3V	5036	FSYSS	6036	FSYSS*
4037	CONTS*	5037	DGND	6037	DGND
4038	FL1R2*	5038	FL1SS	6038	FL1SS*
4039	–2V	5039	FL1RS	6039	FL1RS*
4040	–2V	5040	DGND	6040	DGND
4041	FL2SS*	5041	FL2RS	6041	FL2RS*
4042	FL3R2*	5042	FL3SS	6042	FL3SS*
4043	–5V	5043	DGND	6043	DGND
4044	FL3RS*	5044	FL4SS	6044	FL4SS*
4045	–2V	5045	–2V	6045	–2V
4046	–2V	5046	–2V	6046	–2V
4047	STRT2*	5047	FL4RS	6047	FL4RS*
4048	–5V	5048	DGND	6048	DGND
4049	STRTS*	5049	FBAYS	6049	FBAYS*
4050	CLIN2*	5050	OUTENS	6050	OUTENS*
4051	–2V	5051	DGND	6051	DGND
4052	–2V	5052	CLOUTS	6052	CLOUTS*
4053	–2V	5053	SCSYNC1	6053	SCSYNC1*
4054	RFCLKM*	5054	DGND	6054	DGND
4055	+5V	5055	C00PSM	6055	C00PSM*
4056	ACTRIG*	5056	LTSA2M	6056	LTSA3M
4057	+3V	5057	DGND	6057	DGND
4058	LTSA5M	5058	FAILPSR	6058	FAILPSR*
4059	–2V	5059	FAILENR	6059	IFAILR
4060	–2V	5060	DGND	6060	DGND
4061	–2V	5061	FAIL0LR	6061	FAIL0UR

Table 3.3: TSINT HDI Connector Pinout, Rows 4 – 6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4062	PTSIN*	5062	DGND	6062	DGND
4063	+3V	5063	FAIL1LR	6063	FAIL1UR
4064	–	5064	FAILLM0L	6064	FAILLM0R
4065	+5V	5065	DGND	6065	DGND
4066	CPMENM	5066	FAILLM1L	6066	FAILLM1R
4067	–2V	5067	DPMSDPM	6067	DPMSHDM
4068	–2V	5068	DGND	6068	DGND
4069	–2V	5069	CPMA00M	6069	CPMA01M
4070	CPMA03M	5070	CPMA04M	6070	CPMA05M
4071	CPMA07M	5071	DGND	6071	DGND
4072	+5V	5072	REFOUT1	6072	REFOUT1*
4073	CPMA09M	5073	REFOUT3	6073	REFOUT3*
4074	CPMA11M	5074	DGND	6074	DGND
4075	–2V	5075	DCOMPR	6075	DCOMPR*
4076	–2V	5076	DGND	6076	DGND
4077	–2V	5077	DCIN1	6077	DCIN1*
4078	CPMA13M	5078	DCIN3	6078	DCIN3*
4079	CPMA15M	5079	DGND	6079	DGND
4080	+3V	5080	PSSYNC	6080	PSSYNC*
4081	PTSTH1*	5081	CFPSR	6081	CFPSR*
4082	PTSTH2*	5082	DGND	6082	DGND
4083	–2V	5083	C00PSR	6083	C00PSR*
4084	–2V	5084	LTSA0R	6084	LTSA1R
4085	–2V	5085	DGND	6085	DGND
4086	LTSA2R	5086	LTSA3R	6086	LTSA4R
4087	LTSA5R	5087	FFENR	6087	FFDENR
4088	–5V	5088	DGND	6088	DGND
4089	FFLENR	5089	TGENR	6089	EPENR

Table 3.3: TSINT HDI Connector Pinout, Rows 4 – 6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4090	–2V	5090	–2V	6090	–2V
4091	–2V	5091	–2V	6091	–2V
4092	REFIN*	5092	INITR	6092	WTRIGR
4093	+5V	5093	DGND	6093	DGND
4094	DCOUT*	5094	PBSYR	6094	DPMSDPR
4095	DPMSHDR	5095	DPMLDAR	6095	DPMLLAR
4096	–2V	5096	DGND	6096	DGND
4097	–2V	5097	CPMAENR	6097	CPMA00R
4098	CPMA01R	5098	CPMA02R	6098	CPMA03R
4099	CPMA04R	5099	DGND	6099	DGND
4100	+3V	5100	CPMA05R	6100	CPMA06R
4101	CPMA07R	5101	CPMA08R	6101	CPMA09R
4102	CPMA10R	5102	DGND	6102	DGND
4103	–2V	5103	CPMA11R	6103	CPMA12R
4104	–2V	5104	CPMA13R	6104	CPMA14R
4105	CPMA15R	5105	DGND	6105	DGND
4106	DPMSPSAR	5106	DPMSPSBR	6106	DPMSLABR
4107	+3V	5107	DGND	6107	DGND
4108	DPMSLAAR	5108	DPMS0AR	6108	DPMS0BR
4109	DPMS1AR	5109	DPMS1BR	6109	DPMS2BR
4110	–2V	5110	DGND	6110	DGND
4111	–2V	5111	DPMS2AR	6111	DPMS3BR
4112	DPMS3AR	5112	DPMS4BR	6112	DPMS5BR
4113	DPMS4AR	5113	DGND	6113	DGND
4114	+5V	5114	DPMS5AR	6114	DPMS6BR
4115	DPMS6AR	5115	DPMS7AR	6115	DPMS7BR
4116	–15V	5116	DGND	6116	DGND
4117	–	5117	ACP0AR	6117	ACP0AR*

Table 3.3: TSINT HDI Connector Pinout, Rows 4 – 6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4118	+15V	5118	ACP1AR	6118	ACP1AR*
4119	ACP1M*	5119	DGND	6119	DGND
4120	–2V	5120	ACP0BR	6120	ACP0BR*
4121	–2V	5121	DGND	6121	DGND
4122	ACP0CL*	5122	ACP1BR	6122	ACP1BR*
4123	+3V	5123	ACP0CR	6123	ACP0CR*
4124	ACP1CL*	5124	DGND	6124	DGND
4125	ACP0DR*	5125	ACP1CR	6125	ACP1CR*
4126	–2V	5126	ACP0ER	6125	ACP0ER*
4127	–2V	5127	DGND	6127	DGND
4128	ACP1DR*	5128	ACP1ER	6128	ACP1ER*
4129	ACP1FL*	5129	ACP0FR	6129	ACP0FR*
4130	+5V	5130	DGND	6130	DGND
4131	ACP1GL*	5131	ACP1FR	6131	ACP1FR*
4132	ACP0GR*	5132	ACP1GR	6132	ACP1GR*
4133	DGND	5133	DGND	6133	DGND
4134	ACP0HR*	5134	ACP1HR	6134	ACP1HR*
4135	–5V	5135	–5V	6135	–5V

System Interface

This section describes the signal interface for the TSINT board with the following:

- Trillium Bus Interface on page 3-23
- Digital Backplane Interface on page 3-23
- DWBFNT Interface on page 3-26
- FARMNT Interface on page 3-29
- FLMY/DPRO Interface on page 3-31

Trillium Bus Interface

Table 3.4 shows is a list of the input/output (I/O) Trillium bus interface signals with the Bus Interface NT board (CBIFNT).

Table 3.4: Trillium Bus Signal Interface

Signal	Direction	Description
ADD[2..15]*	Input to TSINT	Address bus for registers.
BUSCK*	Input to TSINT	Trillium bus clock.
READ*	Input to TSINT	Trillium bus read cycle signal.
WRITE*	Input to TSINT	Trillium bus write cycle signal.
EXEC*	Input to TSINT	Autoincrement control used when a read or write is required to cause a pointer to increment.
SCLR,*	Input to TSINT	System master reset.
DAT[0..31*]	Bi-directional	Trillium data bus
BUSY*	Output from TSINT	The busy signal which indicates that a test pattern is running. In continuous pattern mode, the TSINT causes this signal to go false which allows IGTSMD register to be accessed for setting/resetting flags.
CLKSYNC,*	Output from TSINT	Differential 125 MHz clock used to synchronize the CBIFNT with the TSINT.
PSSYNC,*	Output from TSINT	Differential copy of the default C00PS to the CBIFNT.

Digital Backplane Interface

The following is a list of interface signals from and to the Digital Backplane. All of these signals are differential ECL signals and most of them are used for the interlock functions when multiple TSINTs are slaved. The others are used to connect to the PTS and CTMU.

Table 3.5 lists the signal I/O.

Table 3.5: Digital Backplane Signal Interface

Signal	Direction	Description
CONTS,*	Input to TSINT	Differential CONT flag reset signal from the master TSINT.
FL1RS,*	Input to TSINT	Differential Flag 1 reset signal from the master TSINT.

Table 3.5: Digital Backplane Signal Interface (Continued)

Signal	Direction	Description
FL1SS,*	Input to TSINT	Differential Flag1 set signal from the master TSINT.
FL2RS,*	Input to TSINT	Differential Flag 2 reset signal from the master TSINT.
FL2SS,*	Input to TSINT	Differential Flag 2 set signal from the master TSINT.
FL3RS,*	Input to TSINT	Differential Flag 3 reset signal from the master TSINT.
FL3SS,*	Input to TSINT	Differential Flag 3 set signal from the master TSINT.
FBAY[0..2],*	Input to TSINT	Differential fail signal from the slave TSINTs.
INEN[0..2],*	Input to TSINT	Differential fail enable signal from the slave TSINTs. This signal is used to enable the input side of the fail FIFO used by the fail (FBAY) signal from slave TSINTs.
CLIN[0..2],*	Input to TSINT	Differential PS clock from the slave TSINTs associated with the enable(INEN) and fail (FBAY) signals from the slave TSINTs.
FSYSS,*	Input to TSINT	Differential system fail signal from the master TSINT which is sent to the interlock FIFO for the stop on fail function.
OUTENS,*	Input to TSINT	Differential fail enable signal from the master TSINT used to enable the input side of the interlock FIFO for the stop on fail function.
CLOUTS,*	Input to TSINT	Differential PS clock from the master TSINT used by the FSYSS and OUTENS interlock signals.
STRTS,*	Input to TSINT	Differential pattern start signal from the master TSINT.
REFIN,*	Input to TSINT	Differential Reference clock from the master TSINT.
DCIN[0..3],*	Input to TSINT	Differential DCOMP signal to master TSINT from slave TSINTs and the loop back copy from the master TSINT to itself.
PTSIN, *	Input to TSINT	Differential clock input from the programmable VCO synthesizer board.
PTSAIN	Input to TSINT	Single-ended input from the Precision Time Source (PTS).

Table 3.5: Digital Backplane Signal Interface (Continued)

Signal	Direction	Description
CONT[0..2],*	Output from TSINT	Differential Continuous flag reset signal to the slave TSINTs.
FL1S[0..2],*	Output from TSINT	Differential Flag 1 set signal to the slave TSINTs.
FL1R[0..2],*	Output from TSINT	Differential Flag 1 reset signal to the slave TSINTs.
FL2S[0..2],*	Output from TSINT	Differential Flag 2 set signal to the slave TSINTs.
FL2R[0..2],*	Output from TSINT	Differential Flag 2 reset signal to the slave TSINTs.
FL3S[0..2],*	Output from TSINT	Differential Flag 3 set signal to the slave TSINTs.
FL3R[0..2],*	Output from TSINT	Differential Flag 3 reset signal to the slave TSINTs.
FBAYS,*	Output from TSINT	Differential Fail signal for a bay from slave to master TSINT.
INENS,*	Output from TSINT	Differential enable from slave to master TSINT. This signal is used to enable the input side of the fail FIFO used by the fail (FBAYS) signal from slave TSINTs..
CLINS,*	Output from TSINT	Differential PS clock from slave to master TSINT associated with the enable (INENS) and fail (FBAYS) signals.
FSYS[0..2],*	Output from TSINT	Differential system fail signal to the slave TSINTs.
OUTEN[0..2],*	Output from TSINT	Differential enable signal to the slave TSINTs used to enable the input side of the interlock FIFO for the stop on fail function.
CLOUT[0..2],*	Output from TSINT	Differential PS clock to the slave TSINTs used by the FSYS and OUTEN interlock signals.
STRT[0..2],*	Output from TSINT	Differential pattern start signal to the slave TSINTs.
REFOUT[0..3],*	Output from TSINT	Differential Reference clock to the slave TSINTs and the loop back copy from the master TSINT to itself.
DCOUT,*	Output from TSINT	Differential DCOMP signal from slave to master TSINT and loop back copy from master TSINT to itself.

Table 3.5: Digital Backplane Signal Interface (Continued)

Signal	Direction	Description
DPSTRIG, *	Output from TSINT	Differential trigger used by the DUTP current measurement function.
ACCLK0,*	Output from TSINT	Differential ACPMU0 signal to the ACPMU.
ACCLK1,*	Output from TSINT	Differential ACPMU1 signal to the ACPMU.
ACTRIG, *	Output from TSINT	Differential trigger used by the ACPMU.
SCSYNC0,*	Output from TSINT	Differential scope sync used for Test Head 1.
SCSYNC1,*	Output from TSINT	Differential scope sync used for Test Head 2.
PTSTH1, *	Output from TSINT	Differential buffered copy of the PTS reference clock source used by the splitter in Test Head 1.
PTSTH2, *	Output from TSINT	Differential buffered copy of the PTS reference clock source used by the splitter in Test Head 2.

DWBFNT Interface

The TSINT aligns the fail signals from the two DWBFNTs with each other. The fails are received from the DWBFNT on a clock that is equivalent to C00PS.

The synchronized fails are interlocked so that a fail in any test channel will cause all TSINTs to stop in the correct cycle.

Table 3.6 lists the signal I/O.

Table 3.6: DWBFNT Signal Interface

Signal	Direction	Description
FAIL[0..1]LL	Input to TSINT	Fail signals from the DWBFNT for test channels 0–127.
FAILLM[0..1]L	Input to TSINT	Fail signals associated with the FLMYNT for test channels 0–127.
FAILENL	Input to TSINT	Fail enable from the DWBFNT for test channels 0–127.

Table 3.6: DWBFNT Signal Interface (Continued)

Signal	Direction	Description
FAILPSL,*	Input to TSINT	Differential fail clock from the DWBFNT for test channels 0–127; associated with FAIL[0..1]LL, FAIL[0..1]UL, FAILLM[0..1]L and FAILENL.
FAIL[0..1]LR	Input to TSINT	Fail signals from the DWBFNT for test channels 128–255.
FAILLM[0..1]R	Input to TSINT	Fail signals associated with the FLMYNT for test channels 128–255.
FAILENR	Input to TSINT	Fail enable from the DWBFNT for test channels 128–255.
FAILPSR,*	Input to TSINT	Differential fail clock from the DWBFNT for test channels 128–255; associated with FAIL[0..1]LR, FAIL[0..1]UR, FAILLM[0..1]R and FAILENR.
DCOMPL,*	Input to TSINT	Differential buffered version of the DCOMP signal from the DWBFNT for test channels 0–127.
DCOMPR,*	Input to TSINT	Differential buffered version of the DCOMP signal from the DWBFNT for test channels 128–255.
REFCLKL,*	Output from TSINT	Differential copy of the VCO reference clock to the DWBFNT for test channels 0–127.
C00PSL	Output from TSINT	Differential master PS clock to the DWBFNT for test channels 0–127.
INITL	Output from TSINT	Initialization signal to the DWBFNT for test channels 0–127.
PBSYL	Output from TSINT	Pattern busy signal to the DWBFNT for test channels 0–127.
CPMAENL	Output from TSINT	CPM enable to the DWBFNT for test channels 0–127.
CPMA[0..15]L	Output from TSINT	CPMA to the DWBFNT for test channels 0–127.
LTSA[0..5]L	Output from TSINT	Local time set address to the DWBFNT for test channels 0–127.
TGENL	Output from TSINT	Drive side timing generator enable to the DWBFNT for test channels 0–127.
EPENL	Output from TSINT	Extended period enable to the DWBFNT for test channels 0–127.

Table 3.6: DWBFNT Signal Interface (Continued)

Signal	Direction	Description
WTRIGL	Output from TSINT	Waveform trigger enable to the DWBFNT for test channels 0–127.
DPMLDAL	Output from TSINT	DPM load start address signal to the DWBFNT for test channels 0–127.
DPMLLAL	Output from TSINT	DPM load digital send start address signal to the DWBFNT for test channels 0–127.
DPMSDPL	Output from TSINT	DPM step signal to the DWBFNT for test channels 0–127.
DPMSHDL	Output from TSINT	DPM shift signal to the DWBFNT for test channels 0–127.
CFPSL, *	Output from TSINT	Differential fail clock to the DWBFNT for test channels 0–127.
IFAILL	Output from TSINT	Ignore fail to the DWBFNT for test channels 0–127; associated with CFPSL.
FFENL	Output from TSINT	Fail FIFO enable to the DWBFNT (used on FARMNT) for test channels 0–127; associated with CFPSL.
FFDENL	Output from TSINT	Fail FIFO enable to the DWBFNT to control the output of its fail FIFO for test channels 0–127; associated with C00PSL.
FFLENL	Output from TSINT	Fail FIFO enable to the DWBFNT (used on FLMYNT) for test channels 0–127; associated with C00PSL.
REFCLKR,*	Output from TSINT	Differential copy of the VCO reference clock to the DWBFNT for test channels 128–255.
C00PSR	Output from TSINT	Differential master PS clock to the DWBFNT for test channels 128–255.
INITR	Output from TSINT	Initialization signal to the DWBFNT for test channels 128–255.
PBSYR	Output from TSINT	Pattern busy signal to the DWBFNT for test channels 128–255.
CPMAENR	Output from TSINT	CPM enable to the DWBFNT for test channels 128–255.
CPMA[0..15]R	Output from TSINT	CPMA to the DWBFNT for test channels 128–255.
LTSA[0..5]R	Output from TSINT	Local time set address to the DWBFNT for test channels 128–255.

Table 3.6: DWBFNT Signal Interface (Continued)

Signal	Direction	Description
TGENR	Output from TSINT	Drive side timing generator enable to the DWBFNT for test channels 128–255.
EPENR	Output from TSINT	Extended period enable to the DWBFNT for test channels 128–255.
WTRIGR	Output from TSINT	Waveform trigger enable to the DWBFNT for test channels 128–255.
DPMLDAR	Output from TSINT	DPM load start address signal to the DWBFNT for test channels 128–255.
DPMLLAR	Output from TSINT	DPM load digital send start address signal to the DWBFNT for test channels 128–255.
DPMSDPR	Output from TSINT	DPM step signal to the DWBFNT for test channels 128–255.
DPMSHDR	Output from TSINT	DPM shift signal to the DWBFNT for test channels 128–255.
CFPSR, *	Output from TSINT	Differential fail clock to the DWBFNT for test channels 128–255.
IFAILR	Output from TSINT	Ignore fail to the DWBFNT for test channels 128–255; associated with CFPSR.
FFENR	Output from TSINT	Fail FIFO enable to the DWBFNT (used on FARMNT) for test channels 128–255; associated with CFPSR.
FFDENR	Output from TSINT	Fail FIFO enable to the DWBFNT to control the output of its fail FIFO for test channels 128–255; associated with C00PSR.
FFLENR	Output from TSINT	Fail FIFO enable to the DWBFNT (used on FLMYNT) for test channels 128–255; associated with C00PSR.

FARMNT Interface

Table 3.7 lists the I/O signals to and from the FARMNT boards.

Table 3.7: FARMNT SIgnal Interface

Signal	Direction	Description
ACP[0..1]AL,*	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 0–15.
ACP[0..1]BL, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 16–31.

Table 3.7: FARMNT SIgnal Interface (Continued)

Signal	Direction	Description
ACP[0..1]CL, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 32–47.
ACP[0..1]DL, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 48–63.
ACP[0..1]EL, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 64–79.
ACP[0..1]FL, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 80–95.
ACP[0..1]GL, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 96–111.
ACP[0..1]HL,*	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 112–127.
ACP[0..1]AR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 128–143.
ACP[0..1]BR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 144–159.
ACP[0..1]CR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 160–175.
ACP[0..1]DR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 176–191.
ACP[0..1]ER, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 192–207.
ACP[0..1]FR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 208–223.
ACP[0..1]GR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 224–249.
ACP[0..1]HR, *	Input to TSINT	Differential ACPMU bus from the FARMNT for test channels 250–255.
DPMS[0..7]AL	Output from TSINT	DPMA to the FARMNTs for test channels 0–63.
DPMSLAAL	Output from TSINT	Load DPM start address signal used by the DPMS FPGA on the FARMNT.
DPMSPSAL	Output from TSINT	PS clock associated with DPMS[0..7]AL and DPMSLAAL.
DPMS[0..7]BL	Output from TSINT	DPMA to the FARMNTs for test channels 64–127.

Table 3.7: FARMNT SIgnal Interface (Continued)

Signal	Direction	Description
DPMSLABL	Output from TSINT	Load DPM start address signal used by the DPMS FPGA on the FARMNT.
DPMSPSBL	Output from TSINT	PS clock associated with DPMS[0..7]BL and DPMSLABL.
DPMS[0..7]AR	Output from TSINT	DPMA to the FARMNTs for test channels 128–191 and to the TCALNT.
DPMSLAAR	Output from TSINT	Load DPM start address signal used by the DPMS FPGA on the FARMNT.
DPMSPSAR	Output from TSINT	PS clock associated with DPMS[0..7]AR and DPMSLAAR.
DPMS[0..7]BR	Output from TSINT	DPMA to the FARMNTs for test channels 192–255.
DPMSLABR	Output from TSINT	Load DPM start address signal used by the DPMS FPGA on the FARMNT.
DPMSPSBR	Output from TSINT	PS clock associated with DPMS[0..7]BR and DPMSLABR.

FLMY/DPRO Interface

The FLMY and DPRO boards are options for the Fusion HF tester. Table 3.8 lists the I/O signals if either or both boards is installed.

Table 3.8: FLMY/DPRO Signal Interface

Signal	Direction	Description
DPMS[0..7]BL	Output from TSINT	DPMA to the FLMYNT for test channels 0–127.
DPMSLABL	Output from TSINT	Load DPM start address signal used by the FLMYNT.
DPMSPSBL	Output from TSINT	PS clock associated with DPMS[0..7]BL and DPMSLABL.
DPMS[0..7]BR	Output from TSINT	DPMA to the FLMYNT for test channels 128–255.
DPMSLABR	Output from TSINT	Load DPM start address signal used by the FLMYNT.
DPMSPSBR	Output from TSINT	PS clock associated with DPMS[0..7]BR and DPMSLABR.

Buffer Interface NT (CBIFNT)

The Buffer Interface NT (CBIFNT) printed circuit board provides the bus interface between the Digital Crate and the Test Program Accelerator (TPANT), and provides pass-through of the Trillium bus to other crates. One CBIFNT supports 256 test channels: There is one CBIFNT in each Digital Crate.

CBIFNT Functions

The primary functions of the CBIFNT board are:

- Information exchange with TPANT.
- Information exchange with other boards.
- Daisy chaining of buffered data, address and control signals to the other crates.
- Generate clock signals for each system board on the backplane.
- Wire-OR all the interrupts that are of the same type, then write to the status register of CBIFNT.
- Provide an Interrupt Mask/Test registe, to allow the masking of any interrupt signal — except “Thermal Interrupt,” and generate test interrupt signals.
- The “all pin write register” address is fully decoded, then generates the global signal ALLN to all system boards
- For diagnostics, allow the capture of any data or address that is used on the backplane bus. This is used as a read back test.

  For more information on diagnostics, refer to the online manual.

Interface to TPANT

The CBIFNT re-synchronizes the Trillium bus control signals from the TPATNT before passing them on to the other boards in the Digital Crate.

The CBIFNT interfaces to the TPANT through a 32-bit bidirectional data bus and a 16-bit address bus. Communication with TPANT and the next crate is through a differential ECL bus and the communication on the backplane is through a TTL bus.

- CBIFNT receives the following active low TTL signals: INT0N, INT1N, INT2N, INT3N, BUSYN, INTOTEMPN.
- CBIFNT generates the following active low TTL control signals: RDN, WRN, SCLRN, CLK0L-CLK3L, CLK0R-CLK3R, HD1N, HD2N, XECN, ALLN, HPARN, LPARN

Signal Pinout

Table 3.9 lists the pinout of the HDI connector, rows 1–3.

Table 3.9: CBINT HDI Connector Pinout, Rows 1–3

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1001	–5V	2001	–5V	3001	–5V
1002	ADD02*	2002	ADD03*	3002	ADD04*
1003	DGND	2003	DGND	3003	DGND
1004	ADD08*	2004	ADD09*	3004	ADD10*
1005	BUSCK*	2005	ADD14*	3005	ADD15*
1006	n.a.	2006	n.a.	3006	CLKSYNC
1007	DGND	2007	DGND	3007	DGND
1008	BUSY*	2008	TMPWR	3008	DMA*
1009	DAT00*	2009	DAT01*	3009	INT0*
1010	DAT02*	2010	DAT03*	3010	DAT04*
1011	DAT08*	2011	DAT09*	3011	DAT10*
1012	DGND	2012	DGND	3012	DGND
1013	DAT14*	2013	DAT15*	3013	DAT16*
1014	DAT20*	2014	DAT21*	3014	DAT22*
1015	DAT26*	2015	DAT27*	3015	DAT28*
1016	AIN02	2016	AIN02*	3016	–2V
1017	DGND	2017	DGND	3017	n.a.
1018	AIN03	2018	AIN03*	3018	+15V

Table 3.9: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1019	AIN04	2019	AIN04*	3019	AIN05
1020	DGND	2020	DGND	3020	–15V
1021	AIN06	2021	AIN06*	3021	n.a.
1022	AIN07	2022	AIN07*	3022	+5V
1023	DGND	2023	DGND	3023	AIN08
1024	AIN09	2024	AIN09*	3024	AIN10
1025	AIN11	2025	AIN11*	3025	–2V
1026	DGND	2026	DGND	3026	–2V
1027	AIN13	2027	AIN13*	3027	AIN12
1028	AIN14	2028	AIN14*	3028	DIN12*
1029	DGND	2029	DGND	3029	+3V
1030	BSYIN	2030	BSYIN*	3030	AIN15
1031	DGND	2031	DGND	3031	DIN09*
1032	CLRIN	2032	CLRIN*	3032	–2V
1033	WRIN	2033	WRIN*	3033	–2V
1034	DGND	2034	DGND	3034	RDIN
1035	CLKIN	2035	CLKIN*	3035	DIN06*
1036	XECIN	2036	XECIN*	3036	+3V
1037	DGND	2037	DGND	3037	HD2IN
1038	HD1IN	2038	HD1IN*	3038	DIN03*
1039	DMAIN	2039	DMAIN*	3039	–2V
1040	DGND	2040	DGND	3040	–2V
1041	SCKIN	2041	SCKIN*	3041	n.a.
1042	n.a.	2042	n.a.	3042	n.a.
1043	DGND	2043	DGND	3043	+5V
1044	n.a.	2044	n.a.	3044	n.a.
1045	–2V	2045	–2V	3045	–2V
1046	–2V	2046	–2V	3046	–2V
1047	n.a.	2047	n.a.	3047	AOUT02

Table 3.9: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1048	DGND	2048	DGND	3048	–5V
1049	SPBJ31*	2049	SPBJ31	3049	n.a.
1050	PERIN*	2050	PERIN	3050	AOUT05
1051	DGND	2051	DGND	3051	–2V
1052	INTIN*	2052	INTIN	3052	–2V
1053	SPBJ30*	2053	SPBJ30	3053	–2V
1054	DGND	2054	DGND	3054	AOUT09
1055	DIN31*	2055	DIN31	3055	+5V
1056	DIN29*	2056	DIN29	3056	DIN30*
1057	DGND	2057	DGND	3057	+3V
1058	DIN28*	2058	DIN28	3058	AOUT12
1059	DIN27*	2059	DIN27	3059	–2V
1060	DGND	2060	DGND	3060	–2V
1061	DIN26*	2061	DIN26	3061	–2V
1062	DGND	2062	DGND	3062	DIN25*
1063	DIN24*	2063	DIN24	3063	+3V
1064	DIN23*	2064	DIN23	3064	CLROUT
1065	DGND	2065	DGND	3065	+5V
1066	DIN22*	2066	DIN22	3066	n.a.
1067	DIN21*	2067	DIN21	3067	–2V
1068	DGND	2068	DGND	3068	–2V
1069	DIN20*	2069	DIN20	3069	–2V
1070	DIN18*	2070	DIN18	3070	DIN19*
1071	DGND	2071	DGND	3071	HD1OUT
1072	DIN17*	2072	DIN17	3072	+5V
1073	DIN16*	2073	DIN16	3073	n.a.
1074	DGND	2074	DGND	3074	n.a.
1075	n.a.	2075	n.a.	3075	–2V
1076	DGND	2076	DGND	3076	–2V

Table 3.9: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1077	n.a.	2077	n.a.	3077	–2V
1078	n.a.	2078	n.a.	3078	n.a.
1079	DGND	2079	DGND	3079	n.a.
1080	n.a.	2080	n.a.	3080	+3V
1081	n.a.	2081	n.a.	3081	n.a.
1082	DGND	2082	DGND	3082	n.a.
1083	n.a.	2083	n.a.	3083	–2V
1084	SPBJ53*	2084	SPBJ53	3084	–2V
1085	DGND	2085	DGND	3085	–2V
1086	SPBJ52*	2086	SPBJ52	3086	n.a.
1087	ANSELOUT*	2087	ANSELOUT	3087	INTOUT*
1088	DGND	2088	DGND	3088	–5V
1089	DOUT15*	2089	DOUT15	3089	SPBJ50*
1090	–2V	2090	–2V	3090	–2V
1091	–2V	2091	–2V	3091	–2V
1092	DOUT14*	2092	DOUT14	3092	DOUT30*
1093	DGND	2093	DGND	3093	+5V
1094	DOUT12*	2094	DOUT12	3094	DOUT13*
1095	DOUT11*	2095	DOUT11	3095	DOUT27*
1096	DGND	2096	DGND	3096	–2V
1097	DOUT10*	2097	DOUT10	3097	–2V
1098	DOUT08*	2098	DOUT08	3098	DOUT09*
1099	DGND	2099	DGND	3099	DOUT23*
1100	DOUT07*	2100	DOUT07	3100	+3V
1101	DOUT05*	2101	DOUT05	3101	DOUT06*
1102	DGND	2102	DGND	3102	DOUT20*
1103	DOUT04*	2103	DOUT04	3103	–2V
1104	DOUT03*	2104	DOUT03	3104	–2V
1105	DGND	2105	DGND	3105	DOUT02*

Table 3.9: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1106	DOUT01*	2106	DOUT01	3106	n.a.
1107	DGND	2107	DGND	3107	+3V
1108	DOUT00*	2108	DOUT00	3108	n.a.
1109	n.a.	2109	n.a.	3109	n.a.
1110	DGND	2110	DGND	3110	–2V
1111	n.a.	2111	n.a.	3111	–2V
1112	n.a.	2112	n.a.	3112	n.a.
1113	DGND	2113	DGND	3113	n.a.
1114	n.a.	2114	n.a.	3114	+5V
1115	n.a.	2115	n.a.	3115	n.a.
1116	DGND	2116	DGND	3116	–15V
1117	n.a.	2117	n.a.	3117	n.a.
1118	n.a.	2118	n.a.	3118	+15V
1119	DGND	2119	DGND	3119	n.a.
1120	n.a.	2120	n.a.	3120	–2V
1121	DGND	2121	DGND	3121	–2V
1122	n.a.	2122	n.a.	3122	n.a.
1123	n.a.	2123	n.a.	3123	+3V
1124	DGND	2124	DGND	3124	n.a.
1125	n.a.	2125	n.a.	3125	n.a.
1126	n.a.	2126	n.a.	3126	–2V
1127	DGND	2127	DGND	3127	–2V
1128	n.a.	2128	n.a.	3128	n.a.
1129	n.a.	2129	n.a.	3129	n.a.
1130	DGND	2130	DGND	3130	+5V
1131	n.a.	2131	n.a.	3131	n.a.
1132	n.a.	2132	n.a.	3132	n.a.
1133	DGND	2133	DGND	3133	DGND
1134	INTOTMP*	2134	INTOREF	3134	n.a.

Table 3.9: CBINT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1135	–5V	2135	–5V	3135	–5V

Table 3.10 lists the pinout of the HDI connector, rows 4–6.

Table 3.10: CBINT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4001	–5V	5001	–5V	6001	–5V
4002	ADD05*	5002	ADD06*	6002	ADD07*
4003	DGND	5003	DGND	6003	DGND
4004	ADD11*	5004	ADD12*	6004	ADD13*
4005	ALL*	5005	READ*	6005	WRITE*
4006	CLKSYNC*	5006	EXEC*	6006	SCLR*
4007	DGND	5007	DGND	6007	DGND
4008	INTOT*	5008	HEAD01*	6008	HEAD02*
4009	INT1*	5009	INT2*	6009	INT3*
4010	DAT05*	5010	DAT06*	6010	DAT07*
4011	DAT11*	5011	DAT12*	6011	DAT13*
4012	DGND	5012	DGND	6012	DGND
4013	DAT17*	5013	DAT18*	6013	DAT19*
4014	DAT23*	5014	DAT24*	6014	DAT25*
4015	DAT29*	5015	DAT30*	6015	DAT31*
4016	–2V	5016	n.a.	6016	n.a.
4017	n.a.	5017	DGND	6017	DGND
4018	+15V	5018	SPBJ23*	6018	SPBJ23
4019	AIN05*	5019	SPBJ22*	6019	SPBJ22
4020	–15V	5020	DGND	6020	DGND
4021	n.a.	5021	ANSELIN*	6021	ANSELIN
4022	+5V	5022	SPBJ20*	6022	SPBJ20
4023	AIN08*	5023	DGND	6023	DGND
4024	AIN10*	5024	DIN15*	6024	DIN15

Table 3.10: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4025	–2V	5025	DIN14*	6025	DIN14
4026	–2V	5026	DGND	6026	DGND
4027	AIN12*	5027	DIN13*	6027	DIN13
4028	DIN12	5028	DIN11*	6028	DIN11
4029	+3V	5029	DGND	6029	DGND
4030	AIN15*	5030	DIN10*	6030	DIN10
4031	DIN09	5031	DGND	6031	DGND
4032	–2V	5032	DIN08*	6032	DIN08
4033	–2V	5033	DIN07*	6033	DIN07
4034	RDIN*	5034	DGND	6034	DGND
4035	DIN06	5035	DIN05*	6035	DIN05
4036	+3V	5036	DIN04*	6036	DIN04
4037	HD2IN*	5037	DGND	6037	DGND
4038	DIN03	5038	DIN02*	6038	DIN02
4039	–2V	5039	DIN01*	6039	DIN01
4040	–2V	5040	DGND	6040	DGND
4041	n.a.	5041	DIN00*	6041	DIN00
4042	n.a.	5042	n.a.	6042	n.a.
4043	+5V	5043	DGND	6043	DGND
4044	n.a.	5044	n.a.	6044	n.a.
4045	–2V	5045	–2V	6045	–2V
4046	–2V	5046	–2V	6046	–2V
4047	AOUT02*	5047	AOUT03	6047	AOUT03*
4048	–5V	5048	DGND	6048	DGND
4049	n.a.	5049	AOUT04	6049	AOUT04*
4050	AOUT05*	5050	AOUT06	6050	AOUT06*
4051	–2V	5051	DGND	6051	DGND
4052	–2V	5052	AOUT07	6052	AOUT07*
4053	–2V	5053	AOUT08	6053	AOUT08*

Table 3.10: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4054	AOUT09*	5054	DGND	6054	DGND
4055	+5V	5055	AOUT10	6055	AOUT10*
4056	DIN30	5056	AOUT11	6056	AOUT11*
4057	+3V	5057	DGND	6057	DGND
4058	AOUT12*	5058	AOUT13	6058	AOUT13*
4059	–2V	5059	AOUT14	6059	AOUT14*
4060	–2V	5060	DGND	6060	DGND
4061	–2V	5061	AOUT15	6061	AOUT15*
4062	DIN25	5062	DGND	6062	DGND
4063	+3V	5063	BSYOUT	6063	BSYOUT*
4064	CLROUT*	5064	WROUT	6064	WROUT*
4065	+5V	5065	DGND	6065	DGND
4066	n.a.	5066	RDOUT	6066	RDOUT*
4067	–2V	5067	CLKOUT	6067	CLKOUT*
4068	–2V	5068	DGND	6068	DGND
4069	–2V	5069	XECOUT	6069	XECOUT*
4070	DIN19	5070	HD2OUT	6070	HD2OUT*
4071	HD1OUT*	5071	DGND	6071	DGND
4072	+5V	5072	DMAOUT	6072	DMAOUT*
4073	n.a.	5073	SCKOUT	6073	SCKOUT*
4074	n.a.	5074	DGND	6074	DGND
4075	–2V	5075	n.a.	6075	n.a.
4076	–2V	5076	DGND	6076	DGND
4077	–2V	5077	n.a.	6077	n.a.
4078	n.a.	5078	n.a.	6078	n.a.
4079	n.a.	5079	DGND	6079	DGND
4080	+3V	5080	PSSYNC	6080	PSSYNC*
4081	n.a.	5081	n.a.	6081	n.a.
4082	n.a.	5082	DGND	6082	DGND

Table 3.10: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4083	–2V	5083	n.a.	6083	n.a.
4084	–2V	5084	SPBJ61*	6084	SPBJ61
4085	–2V	5085	DGND	6085	DGND
4086	n.a.	5086	PEROUT*	6086	PEROUT
4087	INTOUT	5087	SPBJ60*	6087	SPBJ60
4088	–5V	5088	DGND	6088	DGND
4089	SPBJ50	5089	DOUT31*	6089	DOUT31
4090	–2V	5090	–2V	6090	–2V
4091	–2V	5091	–2V	6091	–2V
4092	DOUT30	5092	DOUT29*	6092	DOUT29
4093	+5V	5093	DGND	6093	DGND
4094	DOUT13	5094	DOUT28*	6094	DOUT28
4095	DOUT27	5095	DOUT26*	6095	DOUT26
4096	–2V	5096	DGND	6096	DGND
4097	–2V	5097	DOUT25*	6097	DOUT25
4098	DOUT09	5098	DOUT24*	6098	DOUT24
4099	DOUT23	5099	DGND	6099	DGND
4100	+3V	5100	DOUT22*	6100	DOUT22
4101	DOUT06	5101	DOUT21*	6101	DOUT21
4102	DOUT20	5102	DGND	6102	DGND
4103	–2V	5103	DOUT19*	6103	DOUT19
4104	–2V	5104	DOUT18*	6104	DOUT18
4105	DOUT02	5105	DGND	6105	DGND
4106	n.a.	5106	DOUT17*	6106	DOUT17
4107	+3V	5107	DGND	6107	DGND
4108	n.a.	5108	DOUT16*	6108	DOUT16
4109	n.a.	5109	n.a.	6109	n.a.
4110	–2V	5110	DGND	6110	DGND
4111	–2V	5111	n.a.	6111	n.a.

Table 3.10: CBINT HDI Connector Pinout, Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4112	n.a.	5112	n.a.	6112	n.a.
4113	n.a.	5113	DGND	6113	DGND
4114	+5V	5114	n.a.	6114	n.a.
4115	n.a.	5115	n.a.	6115	n.a.
4116	–15V	5116	DGND	6116	DGND
4117	n.a.	5117	n.a.	6117	n.a.
4118	+15V	5118	n.a.	6118	n.a.
4119	n.a.	5119	DGND	6119	DGND
4120	n.a.	5120	n.a.	6120	n.a.
4121	–2V	5121	DGND	6121	DGND
4122	n.a.	5122	n.a.	6122	n.a.
4123	+3V	5123	n.a.	6123	n.a.
4124	n.a.	5124	DGND	6124	DGND
4125	n.a.	5125	n.a.	6125	n.a.
4126	–2V	5126	n.a.	6126	n.a.
4127	–2V	5127	DGND	6127	DGND
4128	n.a.	5128	n.a.	6128	n.a.
4129	n.a.	5129	n.a.	6129	n.a.
4130	+5V	5130	DGND	6130	DGND
4131	n.a.	5131	n.a.	6131	n.a.
4132	n.a.	5132	n.a.	6132	n.a.
4133	DGND	5133	DGND	6133	DGND
4134	n.a.	5134	n.a.	6134	n.a.
4135	–5V	5135	–5V	6135	–5V

DW Buffer NT (DWBFNT)

The DW Buffer NT (DWBFNT) printed circuit board interfaces the TSINT board to the FARMNT, DPRO, and FLMY boards in the Digital Crate. Each DWBFNT receives clocks, control signals and address signals from the

TSINT, and buffers these signals to the FARMNT, FLMY, and DPRO boards. DWBFNT also receives fail information from those boards buffers them on to the TSINT.

The DWBFNT supports 128 test channels: One DWBFNT supports 8 FARMNTs. There are two DWFNT boards per Digital Crate, if the crate has more than 8 FARMNTs.

TSINT Interface

The DWBFNT buffers signals to and from the TSINT: fail signals, control and address signals, and reference clocks. Figure 3.6 on page 3-44 shows the signals DWBFNT receives from the TSINT.

Fail Signals

The DWBFNT receives fail information from the FARMNT, FLMY and DPRO boards, and buffers them to the TSINT. To synchronize the fail signals, they are buffered through FIFOs and/or pipelined (re-clocked).

Control and Address Signals

The DWBFNT delivers buffered copies of the control pattern memory (CPM) and data pattern memory (DPM) control and address signals from the TSINT to the FARMNT, FLMY, and DPRO.

CPM. The DWBFNT receives the CPM address (CPMA) and the associated control signals from the TSINT at 125MHz. These signals are delivered to the FLMY and the DPRO at 125MHz.

The signals delivered to FARMNT boards are converted: 125 MHz bus into two parallel 62.5 MHz busses, then buffered and sent to the FARMNT boards. One 62.5 MHz buss contains the CPMA for the even cycles; one buss contains the CPMA for the odd cycles.

DPM. The DPM control signals are processed the same way: 125MHz single buss signals delivered to FLMY and DPRO boards; a pair of 62.5MHz odd/even buss signals delivered to FARMNT boards.

Reference Clocks

The Local Time Set Address (LTSA), a master PSCLK and the voltage controlled oscillator (VCO) reference clock (REFCLK) are received from the TSINT at 125 MHz, and are buffered on a separate 125MHz buss to each FARMNT. An additional copy of the PSCLK and REFCLK are also delivered to the FLMY and the DPRO.

To align all signals, REFCLK signals are delayed. This balances out delay differences in the PSCLK and REFCLK paths.

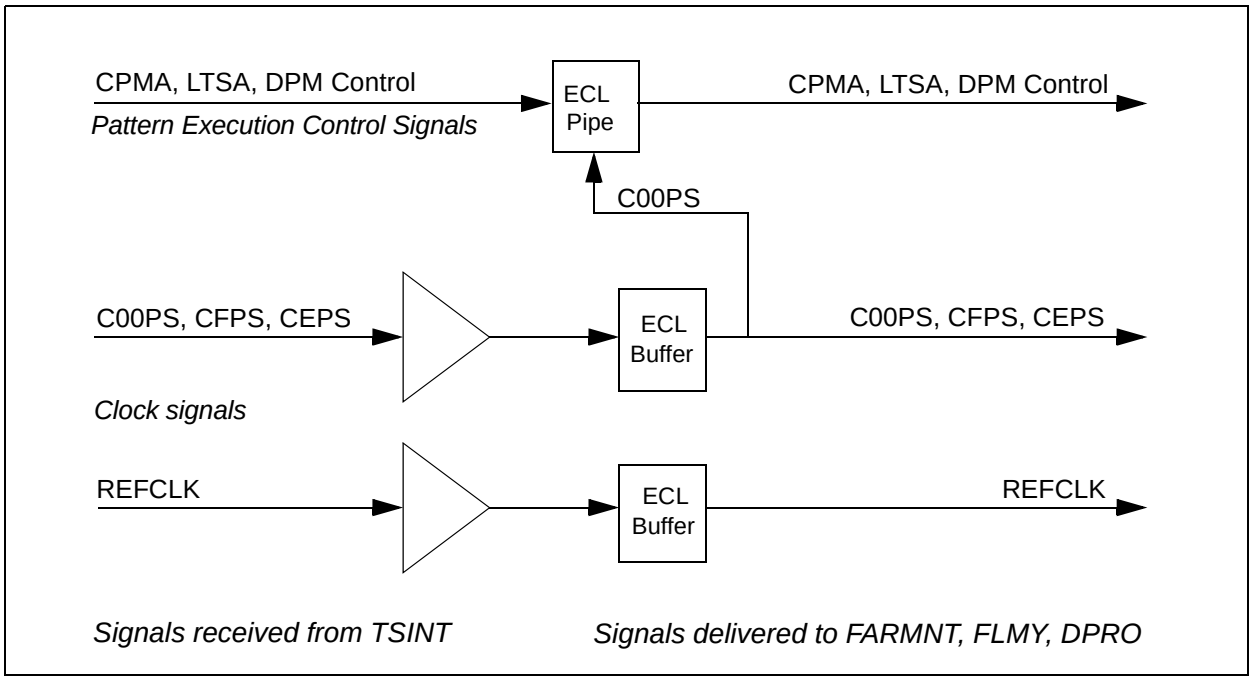


Figure 3.6: Interface to TSINT

Table 3.14 describes the interface signals between DWBFNT and TSINT.

Table 3.11: Signal Interface to TSINT Board

Signal	Description
FAILPS*	The PSCLK that clocks fails from the DWBFNT to the TSINT.
FAILEN	Fail enable signal, delivered with the fails to the TSINT. This signal is synchronized to the FAILPS* from the DWBFNT.
FAIL[0..1]L	The fail bits for the lower 128 pins that are sent to the TSINT. These signals are synchronized to the FAILPS* from the DWBFNT.
FAILLM[0..1]	The fail bits for the FLMYNT, that are sent to the TSINT. These signals are synchronized to the FAILPS* from the DWBFNT.

Table 3.11: Signal Interface to TSINT Board (Continued)

Signal	Description
REFCLK*	The differential copy of the VCO reference clock received from the TSINT.
DCOMP*	The differential comparator output signal sent to the TSINT.
C00PS*	The differential master PSCLK received from the TSINT. This is the earliest PSCLK.
LTSA[0..5]	The local time set address received from the TSINT. These signals are aligned with the C00PS signal, from the TSINT.
FFEN	The fail fifo enable used by the FARMNT, received from the TSINT. This signal is clocked into the DWBFNT by the CFPS from the TSINT.
FFDEN	The fail fifo enable signal used by the DWBFNT to control the output of its fail fifo, received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
TGEN	The drive side timing generator enable received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
EPEN	The extended period enable clock received from the TSINT. This signal is buffered, and fanned out to each FARMNT.
FFLEN	The fail fifo enable used by the FLMYNY to control the output of its fail fifo, received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
WTRIG	The waveform trigger enable received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
INIT	The initial signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
PBSY	The pattern busy signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
DPMSDP	The DPM step signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
DPMSHD	The DPM shift signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
DPMLDA	The DPM load start address signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
DPMLLA	The DPM load digital sent start address signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
CPMAEN	The CPM enable signal received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.
CPMA[00..15]	The CPM address received from the TSINT. This signal is clocked into the DWBFNT by the C00PS from the TSINT.

Table 3.11: Signal Interface to TSINT Board (Continued)

Signal	Description
IFAIL	The ignore-fail bit, received from the TSINT. This signal is piped to the FARMNT boards, and is used to inhibit failures for the DWBFNT's fail log. This signal is aligned with the CFPS clock, from the TSINT.
CFPS*	The fail PS clock, received from the TSINT.

FARMNT Interface

The DWBFNT provides the system clocks and one of the address busses to eight FARMNTs. The remaining control and address signals are sent as two parallel busses running at half rate (62.5MHz). One of the busses carries the even cycle information and the other the odd cycle information.

The FARMNTs send a group of fail and compare signals to the DWBFNT, which are then delivered to the TSINT.

Figure 3.7 on page 3-47 shows the signals DWBFNT delivers to FARMNT boards.

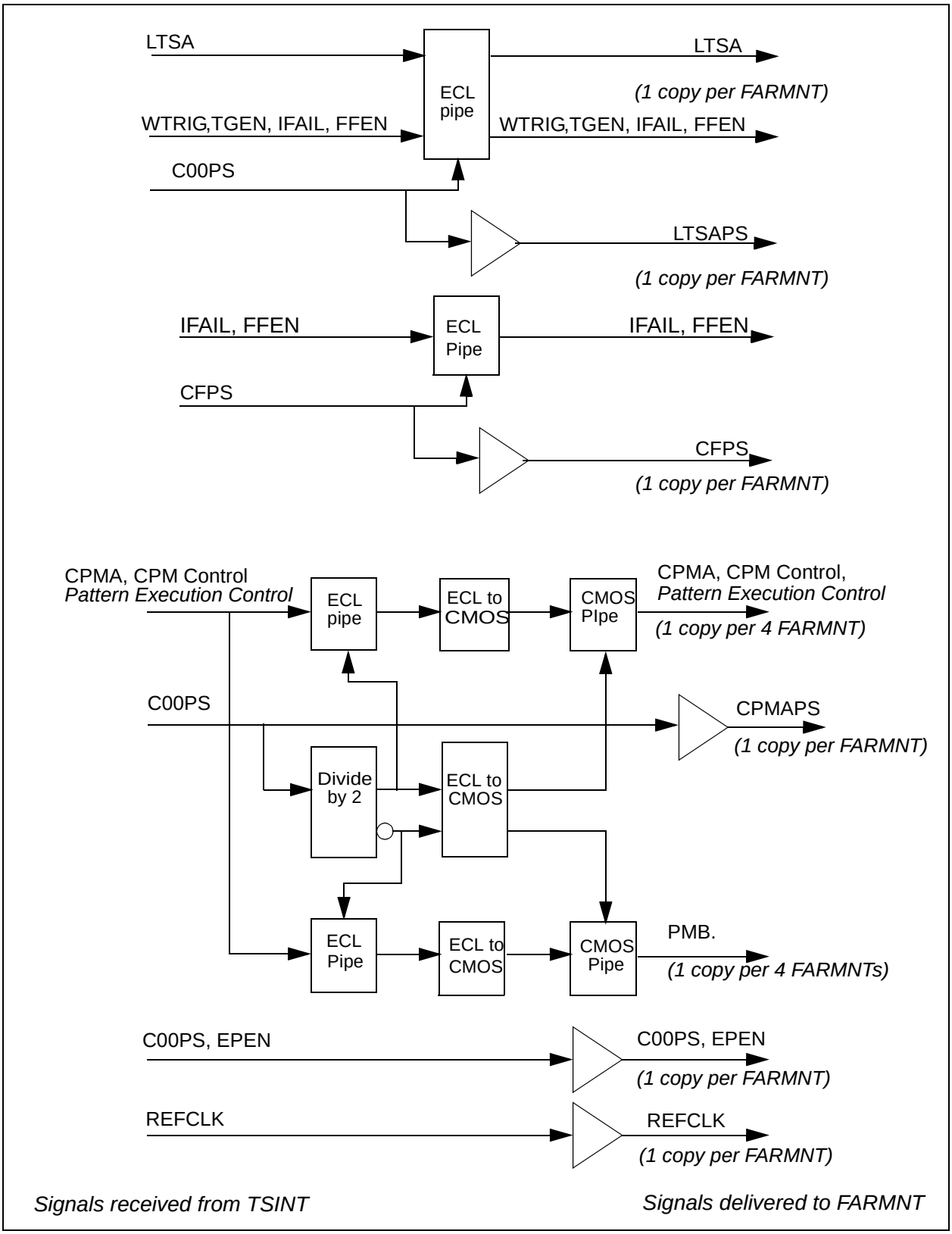


Figure 3.7: Interface to FARMNT

Table 3.14 describes the interface signals between DWBFNT and FARMNT.

Table 3.12: Signal Interface to FARMNT Boards

Signal	Description
LTSAPS[A..H]*	PSCLK: sent to the FARMNTs with the LTSA.
LTSA[0..5][A..H]	The local time set address sent to the FARMNTs: synchronized with the LTSAPS clock.
C00PS[A..H]*	Master PSCLK sent to the FARMNTs.
CFPS[A..H]*	Fail PSCLK sent to the FARMNTs.
REFCLK[A..H]*	VCO reference clock sent to the FARMNTs.
DCOMP[A..H]*	Comparator output signal received from each FARMNT.
FAILPS[A..H]*	The PSCLK that clocks fails on to the DWBFNT from the FARMNTs.
FAILEN[A..H]	Fail enable signals received from the FARMNTs. These signals are aligned with FAILPS[A..H] clocks.
FAIL[0..1][A..H]	Fail signals from the FARMNTs. These signals are aligned with their FAILPS[A..H] clocks.
CPMPS[A..H]*	The PSCLK that clocks all half rate signals on to the FARMNTs.
WTRIG[A..H]	Waveform trigger signal sent to each FARMNT. These signals are synchronized with the C00PS[A..H] clocks.
TGEN[A..H]	The drive time timing generator enable signal sent to each FARMNT. These signals are synchronized with the C00PS[A..H] clocks.
FFEN[A..H]	The fail fifo enable signal sent to each FARMNT. These signals are synchronized with the CFPS[A..H] clocks.
INIT[A..B]	The “A” cycle copy of the initialize signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks. There is no corresponding “B” cycle copy of this signal.
PBSYA	The copy of the pattern busy signal sent to the lower four FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMSDPA[A..B]	The “A” cycle copy of the DPM step signal that is sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMSHDA[A..B]	The “A” cycle copy of the DPM shift signal that is sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.

Table 3.12: Signal Interface to FARMNT Boards (Continued)

Signal	Description
DPMLDAA[A..B]	The "A" cycle copy of the DPM start address load signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMLLAA[A..B]	The "A" cycle copy of the digital send mode start address load signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
CPMAEN[A..B]	The "A" cycle copy of the CPM enable signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
EPEN[A..H]	The extended period enable sent to each of the FARMNTs. These signals are synchronized with the C00PS[A..H] clocks.
CPMA[00..15][A..B]	The "A" cycle copy of the CPM address sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
PBSYB	The copy of the pattern busy signal sent to the upper four FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMSDPB[A..B]	The "B" cycle copy of the DPM step signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMSHDB[A..B]	The "B" cycle copy of the DPM shift signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMLDAB[A..B]	The "B" cycle copy of the DPM start address load signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
DPMLLAB[A..B]	The "B" cycle copy of the digital send mode start address load signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
CPMBEN[A..B]	The "B" cycle copy of the CPM enable signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
CPMB[00..15][A..B]	The "B" cycle copy of the CPM address sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
CYCLB[A..B]	The cycle B signal sent to the FARMNTs. These signals are synchronized with the CPMPS[A..H] clocks.
IFAIL[A..H]	The ignore-fail bits. These signals are synchronized with the CFPS[A..H] clocks.

FLMY and DPRO Interface

DWBFNT interfaces the TSINT to the FLMY and the DPRO, and transfers signals between the FARMNTs, and the FLMY and/or the DPRO. The exchange between the FARMNT, and the FLMY and DPRO is shown in Figure 3.8 on page 3-50.

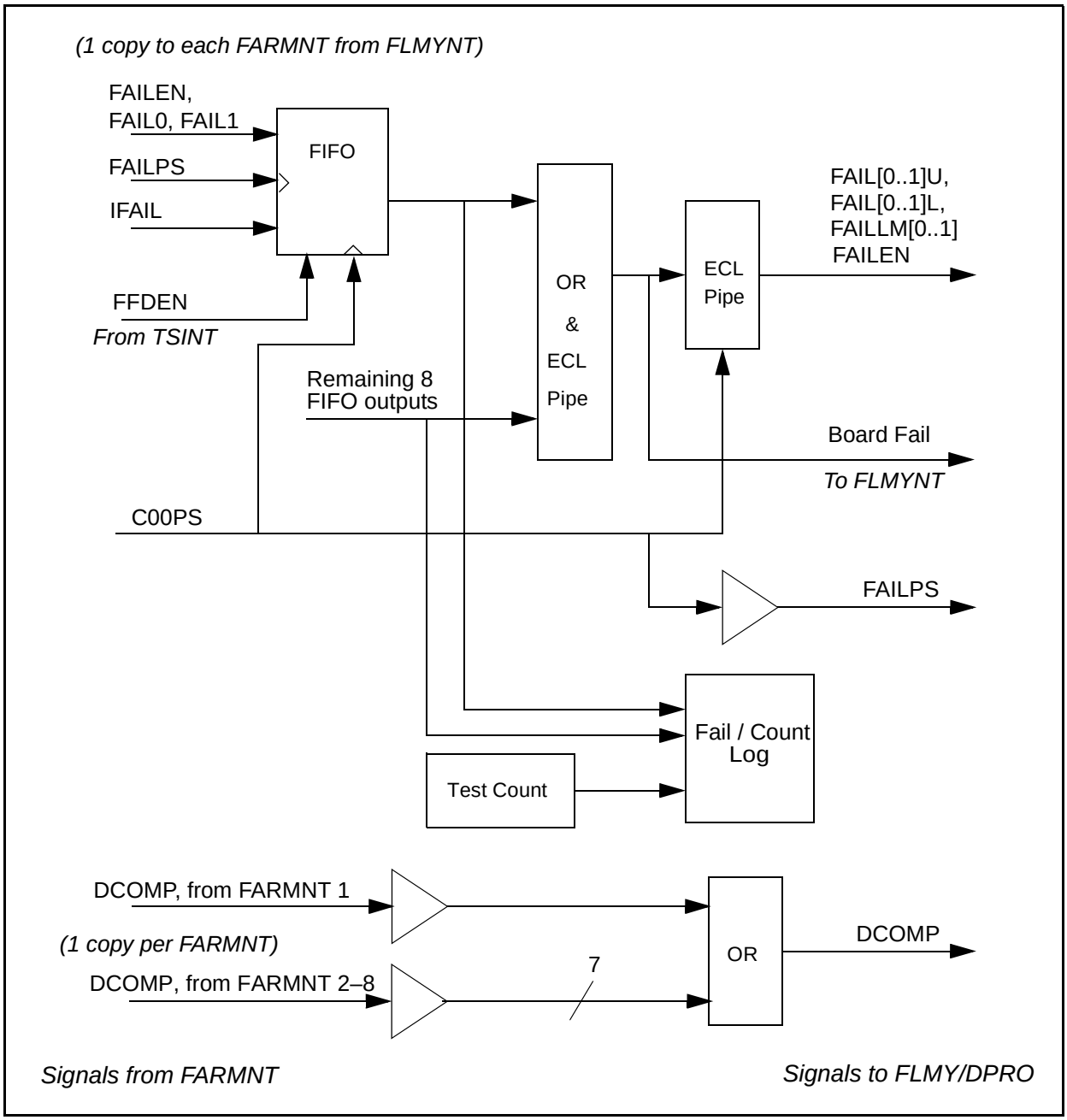


Figure 3.8: Interface to FLMY and DPRO

Table 3.14 describes the interface signals between DWBFNT, and the FLMY and DPRO boards.

Table 3.13: Signal Interface to FLMY and DPRO Boards

Signal	Description
FPSLM,*	The differential PSCLK used to clock the fail bits from the FLMY/DPRO to the DWBFNT.
FENLM	The fail enable signal received from the FLMY/DPRO. This signal is aligned with the FPSLM clock, from the FLMY/DPRO.
FLLM[0..1]	The fail bits received from the FLMY/DPRO. These bits are aligned with the FPSLM clock.
RFCLKLM*	The differential copy of the VCO reference clock delivered to the FLMY/DPRO.
FGPPS*	The differential PSCLK that clocks the 128 pin group fail bit from the DWBFNT to the FLMY/DPRO.
FGPEN	128 pin group fail enable, delivered to the FLMY/DPRO. This signal is aligned with the FGPPS clock.
FAILGP	The 128 pin group fail, delivered to the FLMY/DPRO. This signal is aligned with the FGPPS clock.
C00PSLM*	Copy of the master PSCLK, sent to the FLMY/DPRO.
FFLENLM	The fail fifo enable signal, delivered to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
INITLM	Copy of the initialize signal, delivered to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
PBSYLM	Copy of the pattern busy signal, delivered to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
TGENLM	Copy of the drive time timing generator enable signal, delivered to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
EPENLM	Copy of the extended period enable, delivered to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
DPMSDPLM	Copy of the DPM step signal, sent to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
DPMSHDLM	Copy of the DPM shift signal, sent to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
DPMLDALM	Copy of the DPM start address load signal, delivered to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.

Table 3.13: Signal Interface to FLMY and DPRO Boards

Signal	Description
DPMLLALM	Copy of the digital sent mode start address load signal, sent to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
CPMA[00..15]LM	Copy of the CPMA, sent to the FLMY/DPRO. This signal is synchronized with the C00PSLM clock.
IFAILLM	Ignore-fail bits. These signal is synchronized with the CFPS clock.
CFPSLM	Fail clock, delivered to FLMY/DPRO board.
CPMENLM	CPM enable signal, sent to the FLMY/DPRO. This signal is synchronized with the C00PS clock.

Trillium Bus Interface

Table 3.14 lists the signal interface between the DWBFNT board and the Trillium buss.

Table 3.14: Signal Interface to Trillium Buss

Signal	Description
ADD(02–15)	Register addresses
BUSCK*	Trillium Bus clock
ALL*	All Pin signal: for all pin writes and reads
READ*	Read cycle signal
WRITE*	Write cycle signal
EXEC*	Execute signal: used when the read or write is required for a pointer to increment
SCLR*	The master reset signal
BUSY*	Busy signal
DAT[00–31]*	Data bus signals

For more information, see the appendix Digital Crate on page 3-1.

VX250 Digital Mode

The DWBFNT is to function at up to 125MHz. All support for HFM (High Frequency Mode) is dealt with external to this board by sending this board double wide data at 125 MHz. The CMOS interfaces to this

board are all 62.5 MHz double wide busses. None of these CMOS busses are effected by the choice of either VX125 or VX250 digital modes.

For more information about VX125 and VX250, see Digital Modes on page 1-3.

Fail Signals

The DWBFNT receives fail information from each of the eight FARMNTs, and from the FLMY and/or DPRO that it supports.

Fail Processing

In the VX125 digital mode, the FARMNTs each send two 125 MHz fail signals (A and B), a fail enable signal, and a fail PSCLK to the DWBFNT.

In the VX250 digital mode, for 250MHz operation, the A and B fails become even and odd cycle fails. The DWBFNT logically ORs the eight "A" fail signals, and the eight "B" fail signals, from the eight FARMNTs: 128 test channels.

If fail signals are also received from the FLMY and/or the DPRO – optional boards for the Fusion HF –two "A" and "B" fail signals are received. These are aligned with the two fail "A" and "B" signals from the FARMNTs through a first-in-first-out device (FIFO). This results in four fail signals, which are then delivered to the TSINT. A fail enable and a fail PSCLK accompany the fail signals. This data is transmitted in alternating cycles at the rate of 125MHz each.

Fail Logging

This fail logging is required for datalogging fails when multiple DUTs are tested.

The DWBFNT provides a fail, and fail count logging. This log is used in a log fail only mode. It logs the test count at which a failure occurs, the fail bits from the individual FARMNT boards.

Signal Pinout

Table 3.15 lists the signal pinout of the high density connector (HDI), rows 1–3.

Table 3.15: DWBFNT HDI Connector Pinout Rows 1–3

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1001	–5V	2001	–5V	3001	–5V
1002	ADD02*	2002	ADD03*	3002	ADD04*
1003	DGND	2003	DfaGND	3003	DGND
1004	ADD08*	2004	ADD09*	3004	ADD10*
1005	BUSCK*	2005	ADD14*	3005	ADD15*
1006	n.a.	2006	n.a.	3006	n.a.
1007	DGND	2007	DGND	3007	DGND
1008	BUSY*	2008	TMPWR	3008	DMA*
1009	DAT00*	2009	DAT01*	3009	INT0*
1010	DAT02*	2010	DAT03*	3010	DAT04*
1011	DAT08*	2011	DAT09*	3011	DAT10*
1012	DGND	2012	DGND	3012	DGND
1013	DAT14*	2013	DAT15*	3013	DAT16*
1014	DAT20*	2014	DAT21*	3014	DAT22*
1015	DAT26*	2015	DAT27*	3015	DAT28*
1016	LTSAPSA	2016	LTSAPSA *	3016	–2V
1017	DGND	2017	DGND	3017	TGENA
1018	LTSA0A	2018	LTSA1A	3018	+15V
1019	LTSA2A	2019	LTSA3A	3019	TGENB
1020	DGND	2020	DGND	3020	–15V
1021	LTSA4A	2021	LTSA5A	3021	TGENC
1022	LTSAPSB	2022	LTSAPSB *	3022	+5V
1023	DGND	2023	DGND	3023	TGEND
1024	LTSA0B	2024	LTSA1B	3024	EPENA
1025	LTSA2B	2025	LTSA3B	3025	–2V
1026	DGND	2026	DGND	3026	–2V

Table 3.15: DWBFNT HDI Connector Pinout Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1027	LTSA4B	2027	LTSA5B	3027	EPENB
1028	LTSAPSC	2028	LTSAPSC *	3028	EPENC
1029	DGND	2029	DGND	3029	+3V
1030	LTSA0C	2030	LTSA1C	3030	EPEND
1031	DGND	2031	DGND	3031	C00PSA
1032	LTSA2C	2032	LTSA3C	3032	–2V
1033	LTSA4C	2033	LTSA5C	3033	–2V
1034	DGND	2034	DGND	3034	C00PSH
1035	LTSAPSD	2035	LTSAPSD *	3035	C00PSB
1036	LTSA0D	2036	LTSA1D	3036	+3V
1037	DGND	2037	DGND	3037	C00PSG
1038	LTSA2D	2038	LTSA3D	3038	C00PSC
1039	LTSA4D	2039	LTSA5D	3039	–2V
1040	DGND	2040	DGND	3040	–2V
1041	C00PSD	2041	C00PSD *	3041	C00PSF
1042	CFPSA	2042	CFPSA *	3042	FPSLM
1043	DGND	2043	DGND	3043	+5V
1044	CFPSB	2044	CFPSB *	3044	CFPSF
1045	–2V	2045	–2V	3045	–2V
1046	–2V	2046	–2V	3046	–2V
1047	CFPSC	2047	CFPSC *	3047	CFPSD
1048	DGND	2048	DGND	3048	–5V
1049	REFCLKA	2049	REFCLKA *	3049	FENLM
1050	REFCLKB	2050	REFCLKB *	3050	FLLM0
1051	DGND	2051	DGND	3051	–2V
1052	REFCLKC	2052	REFCLKC *	3052	–2V
1053	REFCLKD	2053	REFCLKD *	3053	–2V
1054	DGND	2054	DGND	3054	RFCLKLM
1055	DCOMPA	2055	DCOMPA *	3055	+5V

Table 3.15: DWBFNT HDI Connector Pinout Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1056	DCOMPB	2056	DCOMPB *	3056	FAILPS
1057	DGND	2057	DGND	3057	+3V
1058	DCOMPC	2058	DCOMPC *	3058	FAILEN
1059	DCOMPD	2059	DCOMPD *	3059	–2V
1060	DGND	2060	DGND	3060	–2V
1061	FAILPSD	2061	FAILPSD *	3061	–2V
1062	DGND	2062	DGND	3062	FAIL0L
1063	FAILEND	2063	FGPEN	3063	+3V
1064	FAIL0D	2064	FAIL1D	3064	FAIL1L
1065	DGND	2065	DGND	3065	+5V
1066	FAILPSC	2066	FAILPSC *	3066	FGPPS
1067	FAILENC	2067	FAILLM0	3067	–2V
1068	DGND	2068	DGND	3068	–2V
1069	FAIL0C	2069	FAIL1C	3069	–2V
1070	FAILPSB	2070	FAILPSB *	3070	n.a.
1071	DGND	2071	DGND	3071	REFCLK
1072	FAILENB	2072	n.a.	3072	+5V
1073	FAIL0B	2073	FAIL1B	3073	FAILPSH
1074	DGND	2074	DGND	3074	FAILPSA
1075	FAILENA	2075	n.a.	3075	–2V
1076	DGND	2076	DGND	3076	–2V
1077	FAIL0A	2077	FAIL1A	3077	–2V
1078	FFENA	2078	FFENB	3078	DCOMP
1079	DGND	2079	DGND	3079	CFPSLM
1080	FFENC	2080	FFEND	3080	+3V
1081	IFAILA	2081	IFAILB	3081	CFPS
1082	DGND	2082	DGND	3082	C00PS
1083	IFAILC	2083	IFAILD	3083	–2V
1084	WTRIGA	2084	WTRIGB	3084	–2V

Table 3.15: DWBFNT HDI Connector Pinout Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1085	DGND	2085	DGND	3085	–2V
1086	WTRIGC	2086	WTRIGD	3086	LTSA0
1087	CPMPSA	2087	CPMPSA *	3087	LTSA2
1088	DGND	2088	DGND	3088	–5V
1089	CPMPSB	2089	CPMPSB *	3089	LTSA4
1090	–2V	2090	–2V	3090	–2V
1091	–2V	2091	–2V	3091	–2V
1092	CPMPSC	2092	CPMPSC *	3092	FFEN
1093	DGND	2093	DGND	3093	+5V
1094	CPMPSD	2094	CPMPSD *	3094	TGEN
1095	n.a.	2095	INITA	3095	FFLEN
1096	DGND	2096	DGND	3096	–2V
1097	PBSYA	2097	DPMSDPAA	3097	–2V
1098	DPMSHDAA	2098	DPMLDAAA	3098	INIT
1099	DGND	2099	DGND	3099	DPMSDP
1100	DPMLLAAA	2100	CPMAENA	3100	+3V
1101	CPMA00A	2101	CPMA01A	3101	DPMLDA
1102	DGND	2102	DGND	3102	n.a.
1103	CPMA02A	2103	CPMA03A	3103	–2V
1104	CPMA04A	2104	CPMA05A	3104	–2V
1105	DGND	2105	DGND	3105	CPMA00
1106	CPMA06A	2106	CPMA07A	3106	CPMA02
1107	DGND	2107	DGND	3107	+3V
1108	CPMA08A	2108	CPMA09A	3108	CPMA04
1109	CPMA10A	2109	CPMA11A	3109	CPMA06
1110	DGND	2110	DGND	3110	–2V
1111	CPMA12A	2111	CPMA13A	3111	–2V
1112	CPMA14A	2112	CPMA15A	3112	CPMA08
1113	DGND	2113	DGND	3113	CPMA10

Table 3.15: DWBFNT HDI Connector Pinout Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1114	DPMSDPBA	2114	DPMSHDBA	3114	+5V
1115	DPMLDABA	2115	DPMLLABA	3115	CPMA12
1116	DGND	2116	DGND	3116	–15V
1117	CYCLBA	2117	CPMBENA	3117	CPMA14
1118	CPMB00A	2118	CPMB01A	3118	+15V
1119	DGND	2119	DGND	3119	C00PSLM
1120	CPMB02A	2120	CPMB03A	3120	–2V
1121	DGND	2121	DGND	3121	–2V
1122	CPMB04A	2122	CPMB05A	3122	IFAILLM
1123	CPMB06A	2123	CPMB07A	3123	+3V
1124	DGND	2124	DGND	3124	INITLM
1125	CPMB08A	2125	CPMB09A	3125	TGENLM
1126	CPMB10A	2126	CPMB11A	3126	–2V
1127	DGND	2127	DGND	3127	–2V
1128	CPMB12A	2128	CPMB13A	3128	DPMSDPLM
1129	CPMB14A	2129	CPMB15A	3129	DPMLDALM
1130	DGND	2130	DGND	3130	+5V
1131	n.a.	2131	CPMENLM	3131	CPMA00LM
1132	CPMA04LM	2132	CPMA05LM	3132	CPMA06LM
1133	DGND	2133	DGND	3133	DGND
1134	CPMA10LM	2134	CPMA11LM	3134	CPMA12LM
1135	–5V	2135	–5V	3135	–5V

Table 3.15 lists the signal pinout of the high density connector (HDI), rows 4–6.

Table 3.16: DWBFNT HDI Connector Pinout Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4001	–5V	5001	–5V	6001	–5V
4002	ADD05*	5002	ADD06*	6002	ADD07*

Table 3.16: DWBFNT HDI Connector Pinout Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4003	DGND	5003	DGND	6003	DGND
4004	ADD11*	5004	ADD12*	6004	ADD13*
4005	ALL*	5005	READ*	6005	WRITE*
4006	n.a.	5006	EXEC*	6006	SCLR*
4007	DGND	5007	DGND	6007	DGND
4008	INTOT*	5008	HEAD01*	6008	HEAD02*
4009	INT1*	5009	INT2*	6009	INT3*
4010	DAT05*	5010	DAT06*	6010	DAT07*
4011	DAT11*	5011	DAT12*	6011	DAT13*
4012	DGND	5012	DGND	6012	DGND
4013	DAT17*	5013	DAT18*	6013	DAT19*
4014	DAT23*	5014	DAT24*	6014	DAT25*
4015	DAT29*	5015	DAT30*	6015	DAT31*
4016	–2V	5016	LTSAPSH	6016	LTSAPSH *
4017	TGENH	5017	DGND	6017	DGND
4018	+15V	5018	LTSA0H	6018	LTSA1H
4019	TGENG	5019	LTSA2H	6019	LTSA3H
4020	–15V	5020	DGND	6020	DGND
4021	TGENF	5021	LTSA4H	6021	LTSA5H
4022	+5V	5022	LTSAPSG	6022	LTSAPSG *
4023	TGENE	5023	DGND	6023	DGND
4024	EPENH	5024	LTSA0G	6024	LTSA1G
4025	–2V	5025	LTSA2G	6025	LTSA3G
4026	–2V	5026	DGND	6026	DGND
4027	EPENG	5027	LTSA4G	6027	LTSA5G
4028	EPENF	5028	LTSAPSF	6028	LTSAPSF *
4029	+3V	5029	DGND	6029	DGND
4030	EPENE	5030	LTSA0F	6030	LTSA1F
4031	C00PSA *	5031	DGND	6031	DGND

Table 3.16: DWBFNT HDI Connector Pinout Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4032	–2V	5032	LTSA2F	6032	LTSA3F
4033	–2V	5033	LTSA4F	6033	LTSA5F
4034	C00PSH *	5034	DGND	6034	DGND
4035	C00PSB *	5035	LTSAPSE	6035	LTSAPSE *
4036	+3V	5036	LTSA0E	6036	LTSA1E
4037	C00PSG *	5037	DGND	6037	DGND
4038	C00PSC *	5038	LTSA2E	6038	LTSA3E
4039	–2V	5039	LTSA4E	6039	LTSA5E
4040	–2V	5040	DGND	6040	DGND
4041	C00PSF *	5041	C00PSE	6041	C00PSE *
4042	FPSLM *	5042	CFPSH	6042	CFPSH *
4043	+5V	5043	DGND	6043	DGND
4044	CFPSF *	5044	CFPSG	6044	CFPSG *
4045	–2V	5045	–2V	6045	–2V
4046	–2V	5046	–2V	6046	–2V
4047	CFPSD *	5047	CFPSE	6047	CFPSE *
4048	–5V	5048	DGND	6048	DGND
4049	n.a.	5049	REFCLKH	6049	REFCLKH *
4050	FLLM1	5050	REFCLKG	6050	REFCLKG *
4051	–2V	5051	DGND	6051	DGND
4052	–2V	5052	REFCLKF	6052	REFCLKF *
4053	–2V	5053	REFCLKE	6053	REFCLKE *
4054	RFCLKLM *	5054	DGND	6054	DGND
4055	+5V	5055	DCOMPH	6055	DCOMPH *
4056	FAILPS *	5056	DCOMPG	6056	DCOMPG *
4057	+3V	5057	DGND	6057	DGND
4058	IFAIL	5058	DCOMPF	6058	DCOMPF *
4059	–2V	5059	DCOMPE	6059	DCOMPE *
4060	–2V	5060	DGND	6060	DGND

Table 3.16: DWBFNT HDI Connector Pinout Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4061	–2V	5061	FAILPSE	6061	FAILPSE *
4062	FAIL0U	5062	DGND	6062	DGND
4063	+3V	5063	FAILENE	6063	FAILGP
4064	FAIL1U	5064	FAIL0E	6064	FAIL1E
4065	+5V	5065	DGND	6065	DGND
4066	FGPPS *	5066	FAILPSF	6066	FAILPSF *
4067	–2V	5067	FAILENF	6067	FAILLM1
4068	–2V	5068	DGND	6068	DGND
4069	–2V	5069	FAIL0F	6069	FAIL1F
4070	n.a.	5070	FAILPSG	6070	FAILPSG *
4071	REFCLK *	5071	DGND	6071	DGND
4072	+5V	5072	FAILENG	6072	n.a.
4073	FAILPSH *	5073	FAIL0G	6073	FAIL1G
4074	FAILPSA *	5074	DGND	6074	DGND
4075	–2V	5075	FAILENH	6075	n.a.
4076	–2V	5076	DGND	6076	DGND
4077	–2V	5077	FAIL0H	6077	FAIL1H
4078	DCOMP *	5078	FFENH	6078	FFENG
4079	CFPSLM *	5079	DGND	6079	DGND
4080	+3V	5080	FFENF	6080	FFENE
4081	CFPS *	5081	IFAILH	6081	IFAILG
4082	C00PS *	5082	DGND	6082	DGND
4083	–2V	5083	IFAILF	6083	IFAILE
4084	–2V	5084	WTRIGH	6084	WTRIGG
4085	–2V	5085	DGND	6085	DGND
4086	LTSA1	5086	WTRIGF	6086	WTRIGE
4087	LTSA3	5087	CPMPSH	6087	CPMPSH *
4088	–5V	5088	DGND	6088	DGND
4089	LTSA5	5089	CPMPSG	6089	CPMPSG *

Table 3.16: DWBFNT HDI Connector Pinout Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4090	–2V	5090	–2V	6090	–2V
4091	–2V	5091	–2V	6091	–2V
4092	FFDEN	5092	CPMPSF	6092	CPMPSF *
4093	+5V	5093	DGND	6093	DGND
4094	EPEN	5094	CPMPSE	6094	CPMPSE *
4095	WTRIG	5095	n.a.	6095	INITB
4096	–2V	5096	DGND	6096	DGND
4097	–2V	5097	PBSYB	6097	DPMSDPAB
4098	PBSY	5098	DPMSHDAB	6098	DPMLDAAB
4099	DPMSHD	5099	DGND	6099	DGND
4100	+3V	5100	DPMLLAAB	6100	CPMAENB
4101	DPMLLA	5101	CPMA00B	6101	CPMA01B
4102	CPMAEN	5102	DGND	6102	DGND
4103	–2V	5103	CPMA02B	6103	CPMA03B
4104	–2V	5104	CPMA04B	6104	CPMA05B
4105	CPMA01	5105	DGND	6105	DGND
4106	CPMA03	5106	CPMA06B	6106	CPMA07B
4107	+3V	5107	DGND	6107	DGND
4108	CPMA05	5108	CPMA08B	6108	CPMA09B
4109	CPMA07	5109	CPMA10B	6109	CPMA11B
4110	–2V	5110	DGND	6110	DGND
4111	–2V	5111	CPMA12B	6111	CPMA13B
4112	CPMA09	5112	CPMA14B	6112	CPMA15B
4113	CPMA11	5113	DGND	6113	DGND
4114	+5V	5114	DPMSDPBB	6114	DPMSHDBB
4115	CPMA13	5115	DPMLDABB	6115	DPMLLABB
4116	–15V	5116	DGND	6116	DGND
4117	CPMA15	5117	CYCLBB	6117	CPMBENB
4118	+15V	5118	CPMB00B	6118	CPMB01B

Table 3.16: DWBFNT HDI Connector Pinout Rows 4–6 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4119	C00PSLM *	5119	DGND	6119	DGND
4120	–2V	5120	CPMB02B	6120	CPMB03B
4121	–2V	5121	DGND	6121	DGND
4122	FFLENLM	5122	CPMB04B	6122	CPMB05B
4123	+3V	5123	CPMB06B	6123	CPMB07B
4124	PBSYLM	5124	DGND	6124	DGND
4125	EPENLM	5125	CPMB08B	6125	CPMB09B
4126	–2V	5126	CPMB10B	6126	CPMB11B
4127	–2V	5127	DGND	6127	DGND
4128	DPMSHDLM	5128	CPMB12B	6128	CPMB13B
4129	DPMLLALM	5129	CPMB14B	6129	CPMB15B
4130	+5V	5130	DGND	6130	DGND
4131	CPMA01LM	5131	CPMA02LM	6131	CPMA03LM
4132	CPMA07LM	5132	CPMA08LM	6132	CPMA09LM
4133	DGND	5133	DGND	6133	DGND
4134	CPMA13LM	5134	CPMA14LM	6134	CPMA15LM
4135	–5V	5135	–5V	6135	–5V

Diagnostics

This board provides read back of the high speed data input and output busses. This allows the diagnostics to verify that the correct data is both entering and leaving the board.

Format Response Memory NT (FARMNT)

The FARMNT printed circuit boards are located in the Fusion HF Digital Crate. One FARMNT board supports 16 test channels. For each test channel, the board contains the user-defined test pattern and timing information, and the timing generators that generate the user's programmed wave forms.

The test patterns are stored in the control pattern memory (CPM) and the data pattern memory (DPM). For more information about CPM and DPM, refer to Pattern Memory Loading on page 5-6, Test Pattern Timing Control on page 6-6, Waveform and Algorithmic Patterns on page 4-1.

In the VX125 digital mode, FARMNT operates at rates of up to 125 MHz. In the VX250 mode, wave forms run up to 250MHz. For more information about digital modes, refer to Digital Modes on page 1-3.

High Speed Interface

The high speed interface is delivering test patterns to the test head, and receiving signals from the test head. The results from the test head are forwarded to the DWBFNT, which then forwards the data to the TSINT.

Test Patterns

The FARMNT receives the control and address signals directly from the DWBFNT. These signals control the start-up and shut down of the timing generators, and provide CPM and DPM address and control information.

The FARMNT delivers drive and I/O signals, test pattern signals, to the Fusion HF test head.

Compare Signals

The FARMNT receives the compare result signals from the test heads, and both compare and fail signals from other boards in the Digital Crate.

The compare signals are delivered to the DWBFNT board, and to the FLMY and/or DPRO boards (if the options are installed). All compare signals are delivered to the DWBFNT.

Fail Signals

The FARMNT delivers fail signals to the DWBFNT board, and if the following options are installed, to the FLMY board and/or the DPRO board.

DWBFNT Fail Path. The fail path to the DWBFNT is two bits wide per test channel, and operates up to 125 MHz.

The fail signals themselves are produced by logically ORing the test channel fail signals, which supports masking the fail bits from individual test channels. This function is also used by the optional boards, FLMY and DPRO.

FLMY/DPRO Fail Path. In VX125 digital mode, the fail path to the DWBFNT is two bits wide and runs at rate of up to 125 MHz. Under normal operating conditions one of these bits per pin is used for even cycle failures and the other for odd cycle failures.

If the system is operating the VX250 mode, one bit is used for the failures from the first half of the tester cycle and the other bit for the failures from the second half of the tester cycle.

In the VX250 mode, a single test cycle is split into two. This allows the frequency to double to 250 MHz.

Reference Clock

The FARMNT receives a REFCLK (32.25 MHz) from the DWBFNT. REFCLK provides the reference signal for a 125 MHz voltage controlled oscillator (VCO).

The REFCLK drives the phase shifter for the PSCLK.

PSCLK

The FARMNT receives several phases of the reference clock (PSCLK) from the DWBFNT, including a "master" PSCLK.

The PSCLK reclocks the following:

- CPMA control signals
- DPMA control signals

The phase shifted PSCLK delays the following:

- Drive signals
- Compare signals
- Period Accumulate Value (PAV)
  PAV adjusts the duration of period values when necessary.

Sync Clock

The FARMNT provides a sync clock to provide an additional PSCLK to the timing generator. The timing is set by the local time set address (LTSA) from the DWBFNT board.

Trillium Bus Interface

The registers on the FARMNT are accessible through the Trillium Bus Interface. This interface is a 32 bit data bus with a 16 bit address bus.

For detailed information about registers, refer to the Register Data Base Utility (RDBU

For more information about the Trillium Bus, refer to Bus Interface on page 2-1.

Connector Pinout

Table 3.17 lists the pinout for the high density interface (HDI) connector, rows 1–3.

Table 3.17: FARMNT HDI Connector Pinout, Rows 1–3

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1001	–5V	2001	–5V	3001	–5V
1002	ADD02*	2002	ADD03*	3002	ADD04*
1003	DGND	2003	DGND	3003	DGND
1004	ADD08*	2004	ADD09*	3004	ADD10*
1005	BUSCK*	2005	ADD14*	3005	ADD15*
1006	n.a.	2006	n.a.	3006	n.a.
1007	DGND	2007	DGND	3007	DGND
1008	BUSY*	2008	TMPWR	3008	DMA*
1009	DAT00*	2009	DAT01*	3009	INT0*
1010	DAT02*	2010	DAT03*	3010	DAT04*
1011	DAT08*	2011	DAT09*	3011	DAT10*
1012	DGND	2012	DGND	3012	DGND
1013	DAT14*	2013	DAT15*	3013	DAT16*
1014	DAT20*	2014	DAT21*	3014	DAT22*

Table 3.17: FARMNT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1015	DAT26*	2015	DAT27*	3015	DAT28*
1016	n.a.	2016	n.a.	3016	–2V
1017	DGND	2017	DGND	3017	LTSAPS
1018	H1DRE000	2018	H2DRE000	3018	+15V
1019	H1DRE000*	2019	H2DRE000*	3019	LTSA0
1020	DGND	2020	DGND	3020	–15V
1021	H1DAT000*	2021	H2DAT000*	3021	LTSA2
1022	H1DAT000	2022	H2DAT000	3022	+5V
1023	DGND	2023	DGND	3023	LTSA4
1024	H1HRS000*	2024	H2HRS000*	3024	n.a.
1025	H1HRS000	2025	H2HRS000	3025	–2V
1026	DGND	2026	DGND	3026	–2V
1027	H1LRS000	2027	H2LRS000	3027	CEPS
1028	H1LRS000*	2028	H2LRS000*	3028	C00PS
1029	DGND	2029	DGND	3029	+3V
1030	n.a.	2030	n.a.	3030	CFPS
1031	DGND	2031	DGND	3031	n.a.
1032	H1DRE002	2032	H2DRE002	3032	–2V
1033	H1DRE002*	2033	H2DRE002*	3033	–2V
1034	DGND	2034	DGND	3034	REFCLK
1035	H1DAT002*	2035	H2DAT002*	3035	n.a.
1036	H1DAT002	2036	H2DAT002	3036	+3V
1037	DGND	2037	DGND	3037	DCOMP
1038	H1HRS002*	2038	H2HRS002*	3038	FAILPS
1039	H1HRS002	2039	H2HRS002	3039	–2V
1040	DGND	2040	DGND	3040	–2V
1041	H1LRS002	2041	H2LRS002	3041	FAILEN
1042	H1LRS002*	2042	H2LRS002*	3042	FAIL0
1043	DGND	2043	DGND	3043	+5V

Table 3.17: FARMNT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1044	n.a.	2044	n.a.	3044	n.a.
1045	–2V	2045	–2V	3045	–2V
1046	–2V	2046	–2V	3046	–2V
1047	n.a.	2047	n.a.	3047	FLMPS
1048	DGND	2048	DGND	3048	–5V
1049	H1DRE004	2049	H2DRE004	3049	FLMEN
1050	H1DRE004*	2050	H2DRE004*	3050	FA00
1051	DGND	2051	DGND	3051	–2V
1052	H1DAT004*	2052	H2DAT004*	3052	–2V
1053	H1DAT004	2053	H2DAT004	3053	–2V
1054	DGND	2054	DGND	3054	FA01
1055	H1HRS004*	2055	H2HRS004*	3055	+5V
1056	H1HRS004	2056	H2HRS004	3056	FA02
1057	DGND	2057	DGND	3057	+3V
1058	H1LRS004	2058	H2LRS004	3058	FA03
1059	H1LRS004*	2059	H2LRS004*	3059	–2V
1060	DGND	2060	DGND	3060	–2V
1061	n.a.	2061	n.a.	3061	–2V
1062	DGND	2062	DGND	3062	FA04
1063	H1DRE006	2063	H2DRE006	3063	+3V
1064	H1DRE006*	2064	H2DRE006*	3064	FA05
1065	DGND	2065	DGND	3065	+5V
1066	H1DAT006*	2066	H2DAT006*	3066	FA06
1067	H1DAT006	2067	H2DAT006	3067	–2V
1068	DGND	2068	DGND	3068	–2V
1069	H1HRS006*	2069	H2HRS006*	3069	–2V
1070	H1HRS006	2070	H2HRS006	3070	FA07
1071	DGND	2071	DGND	3071	FA08
1072	H1LRS006	2072	H2LRS006	3072	+5V

Table 3.17: FARMNT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1073	H1LRS006*	2073	H2LRS006*	3073	FA09
1074	DGND	2074	DGND	3074	FA10
1075	n.a.	2075	n.a.	3075	–2V
1076	DGND	2076	DGND	3076	–2V
1077	H1DRE008	2077	H2DRE008	3077	–2V
1078	H1DRE008*	2078	H2DRE008*	3078	FA11
1079	DGND	2079	DGND	3079	FA12
1080	H1DAT008*	2080	H2DAT008*	3080	+3V
1081	H1DAT008	2081	H2DAT008	3081	FA13
1082	DGND	2082	DGND	3082	FA14
1083	H1HRS008*	2083	H2HRS008*	3083	–2V
1084	H1HRS008	2084	H2HRS008	3084	–2V
1085	DGND	2085	DGND	3085	–2V
1086	H1LRS008	2086	H2LRS008	3086	FA15
1087	H1LRS008*	2087	H2LRS008*	3087	CPMPS
1088	DGND	2088	DGND	3088	–5V
1089	WTRIGA	2089	TGENDA	3089	TGENRA
1090	–2V	2090	–2V	3090	–2V
1091	–2V	2091	–2V	3091	–2V
1092	DPMSDPA	2092	DPMSHDA	3092	DPMLDAA
1093	DGND	2093	DGND	3093	+5V
1094	H1DRE010	2094	H2DRE010	3094	CPMA00
1095	H1DRE010*	2095	H2DRE010*	3095	CPMA02
1096	DGND	2096	DGND	3096	–2V
1097	H1DAT010*	2097	H2DAT010*	3097	–2V
1098	H1DAT010	2098	H2DAT010	3098	CPMA04
1099	DGND	2099	DGND	3099	CPMA06
1100	H1HRS010*	2100	H2HRS010*	3100	+3V
1101	H1HRS010	2101	H2HRS010	3101	CPMA08

Table 3.17: FARMNT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1102	DGND	2102	DGND	3102	CPMA10
1103	H1LRS010	2103	H2LRS010	3103	–2V
1104	H1LRS010*	2104	H2LRS010*	3104	–2V
1105	DGND	2105	DGND	3105	CPMA12
1106	WTRIGB	2106	TGENDB	3106	CPMA14
1107	DGND	2107	DGND	3107	+3V
1108	H1DRE012	2108	H2DRE012	3108	FFENB
1109	H1DRE012*	2109	H2DRE012*	3109	DPMSDPB
1110	DGND	2110	DGND	3110	–2V
1111	H1DAT012*	2111	H2DAT012*	3111	–2V
1112	H1DAT012	2112	H2DAT012	3112	DPMLDAB
1113	DGND	2113	DGND	3113	CYCLB
1114	H1HRS012*	2114	H2HRS012*	3114	+5V
1115	H1HRS012	2115	H2HRS012	3115	CPMB00
1116	DGND	2116	DGND	3116	–15V
1117	H1LRS012	2117	H2LRS012	3117	CPMB02
1118	H1LRS012*	2118	H2LRS012*	3118	+15V
1119	DGND	2119	DGND	3119	CPMB04
1120	CPMB06	2120	CPMB07	3120	–2V
1121	DGND	2121	DGND	3121	–2V
1122	H1DRE014	2122	H2DRE014	3122	CPMB10
1123	H1DRE014*	2123	H2DRE014*	3123	+3V
1124	DGND	2124	DGND	3124	CPMB12
1125	H1DAT014*	2125	H2DAT014*	3125	CPMB14
1126	H1DAT014	2126	H2DAT014	3126	–2V
1127	DGND	2127	DGND	3127	–2V
1128	H1HRS014*	2128	H2HRS014*	3128	DPMSPS
1129	H1HRS014	2129	H2HRS014	3129	DPMS0
1130	DGND	2130	DGND	3130	+5V

Table 3.17: FARMNT HDI Connector Pinout, Rows 1–3 (Continued)

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1131	H1LRS014	2131	H2LRS014	3131	DPMS2
1132	H1LRS014*	2132	H2LRS014*	3132	DPMS4
1133	DGND	2133	DGND	3133	DGND
1134	ACP0	2134	ACP0 FS	3134	DPMS6
1135	–5V	2135	–5V	3135	–5V

Table 3.18 lists the pinout of the HDI connector, rows 4–6.

Table 3.18: FARMNT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4001	–5V	5001	–5V	6001	–5V
4002	ADD05*	5002	ADD06*	6002	ADD07*
4003	DGND	5003	DGND	6003	DGND
4004	ADD11*	5004	ADD12*	6004	ADD13*
4005	ALL*	5005	READ*	6005	WRITE*
4006	n.a.	5006	EXEC*	6006	SCLR*
4007	DGND	5007	DGND	6007	DGND
4008	INTOT*	5008	HEAD01*	6008	HEAD02*
4009	INT1*	5009	INT2*	6009	INT3*
4010	DAT05*	5010	DAT06*	6010	DAT07*
4011	DAT11*	5011	DAT12*	6011	DAT13*
4012	DGND	5012	DGND	6012	DGND
4013	DAT17*	5013	DAT18*	6013	DAT19*
4014	DAT23*	5014	DAT24*	6014	DAT25*
4015	DAT29*	5015	DAT30*	6015	DAT31*
4016	–2V	5016	n.a.	6016	n.a.
4017	LTSAPS *	5017	DGND	6017	DGND
4018	+15V	5018	H1DAT001	6018	H2DAT001
4019	LTSA1	5019	H1DAT001*	6019	H2DAT001*
4020	–15V	5020	DGND	6020	DGND

Table 3.18: FARMNT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4021	LTSA3	5021	H1DRE001*	6021	H2DRE001*
4022	+5V	5022	H1DRE001	6022	H2DRE001
4023	LTSA5	5023	DGND	6023	DGND
4024	n.a.	5024	H1LRS001*	6024	H2LRS001*
4025	–2V	5025	H1LRS001	6025	H2LRS001
4026	–2V	5026	DGND	6026	DGND
4027	CEPS *	5027	H1HRS001	6027	H2HRS001
4028	C00PS	5028	H1HRS001*	6028	H2HRS001*
4029	+3V	5029	DGND	6029	DGND
4030	CFPS *	5030	n.a.	6030	n.a.
4031	n.a.	5031	DGND	6031	DGND
4032	–2V	5032	H1DAT003	6032	H2DAT003
4033	–2V	5033	H1DAT003*	6033	H2DAT003*
4034	REFCLK *	5034	DGND	6034	DGND
4035	n.a.	5035	H1DRE003*	6035	H2DRE003*
4036	+3V	5036	H1DRE003	6036	H2DRE003
4037	DCOMP *	5037	DGND	6037	DGND
4038	FAILPS *	5038	H1LRS003*	6038	H2LRS003*
4039	–2V	5039	H1LRS003	6039	H2LRS003
4040	–2V	5040	DGND	6040	DGND
4041	n.a.	5041	H1HRS003	6041	H2HRS003
4042	FAIL1	5042	H1HRS003*	6042	H2HRS003*
4043	+5V	5043	DGND	6043	DGND
4044	n.a.	5044	n.a.	6044	n.a.
4045	–2V	5045	–2V	6045	–2V
4046	–2V	5046	–2V	6046	–2V
4047	FLMPS *	5047	n.a.	6047	n.a.
4048	–5V	5048	DGND	6048	DGND
4049	n.a.	5049	H1DAT005	6049	H2DAT005

Table 3.18: FARMNT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4050	FB00	5050	H1DAT005*	6050	H2DAT005*
4051	–2V	5051	DGND	6051	DGND
4052	–2V	5052	H1DRE005*	6052	H2DRE005*
4053	–2V	5053	H1DRE005	6053	H2DRE005
4054	FB01	5054	DGND	6054	DGND
4055	+5V	5055	H1LRS005*	6055	H2LRS005*
4056	FB02	5056	H1LRS005	6056	H2LRS005
4057	+3V	5057	DGND	6057	DGND
4058	FB03	5058	H1HRS005	6058	H2HRS005
4059	–2V	5059	H1HRS005*	6059	H2HRS005*
4060	–2V	5060	DGND	6060	DGND
4061	–2V	5061	n.a.	6061	n.a.
4062	FB04	5062	DGND	6062	DGND
4063	+3V	5063	H1DAT007	6063	H2DAT007
4064	FB05	5064	H1DAT007*	6064	H2DAT007*
4065	+5V	5065	DGND	6065	DGND
4066	FB06	5066	H1DRE007*	6066	H2DRE007*
4067	–2V	5067	H1DRE007	6067	H2DRE007
4068	–2V	5068	DGND	6068	DGND
4069	–2V	5069	H1LRS007*	6069	H2LRS007*
4070	FB07	5070	H1LRS007	6070	H2LRS007
4071	FB08	5071	DGND	6071	DGND
4072	+5V	5072	H1HRS007	6072	H2HRS007
4073	FB09	5073	H1HRS007*	6073	H2HRS007*
4074	FB10	5074	DGND	6074	DGND
4075	–2V	5075	n.a.	6075	n.a.
4076	–2V	5076	DGND	6076	DGND
4077	–2V	5077	H1DAT009	6077	H2DAT009
4078	FB11	5078	H1DAT009*	6078	H2DAT009*

Table 3.18: FARMNT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4079	FB12	5079	DGND	6079	DGND
4080	+3V	5080	H1DRE009*	6080	H2DRE009*
4081	FB13	5081	H1DRE009	6081	H2DRE009
4082	FB14	5082	DGND	6082	DGND
4083	–2V	5083	H1LRS009*	6083	H2LRS009*
4084	–2V	5084	H1LRS009	6084	H2LRS009
4085	–2V	5085	DGND	6085	DGND
4086	FB15	5086	H1HRS009	6086	H2HRS009
4087	CPMPS *	5087	H1HRS009*	6087	H2HRS009*
4088	–5V	5088	DGND	6088	DGND
4089	FFENA	5089	INIT	6089	PBSY
4090	–2V	5090	–2V	6090	–2V
4091	–2V	5091	–2V	6091	–2V
4092	DPMLLAA	5092	EPENA	6092	CPMAEN
4093	+5V	5093	DGND	6093	DGND
4094	CPMA01	5094	H1DAT011	6094	H2DAT011
4095	CPMA03	5095	H1DAT011*	6095	H2DAT011*
4096	–2V	5096	DGND	6096	DGND
4097	–2V	5097	H1DRE011*	6097	H2DRE011*
4098	CPMA05	5098	H1DRE011	6098	H2DRE011
4099	CPMA07	5099	DGND	6099	DGND
4100	+3V	5100	H1LRS011*	6100	H2LRS011*
4101	CPMA09	5101	H1LRS011	6101	H2LRS011
4102	CPMA11	5102	DGND	6102	DGND
4103	–2V	5103	H1HRS011	6103	H2HRS011
4104	–2V	5104	H1HRS011*	6104	H2HRS011*
4105	CPMA13	5105	DGND	6105	DGND
4106	CPMA15	5106	TGENRB	6106	n.a.
4107	+3V	5107	DGND	6107	DGND

Table 3.18: FARMNT HDI Connector Pinout, Rows 4–6

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
4108	EPENB	5108	H1DAT013	6108	H2DAT013
4109	DPMSHDB	5109	H1DAT013*	6109	H2DAT013*
4110	–2V	5110	DGND	6110	DGND
4111	–2V	5111	H1DRE013*	6111	H2DRE013*
4112	DPMLLAB	5112	H1DRE013	6112	H2DRE013
4113	CPMBEN	5113	DGND	6113	DGND
4114	+5V	5114	H1LRS013*	6114	H2LRS013*
4115	CPMB01	5115	H1LRS013	6115	H2LRS013
4116	–15V	5116	DGND	6116	DGND
4117	CPMB03	5117	H1HRS013	6117	H2HRS013
4118	+15V	5118	H1HRS013*	6118	H2HRS013*
4119	CPMB05	5119	DGND	6119	DGND
4120	–2V	5120	CPMB08	6120	CPMB09
4121	–2V	5121	DGND	6121	DGND
4122	CPMB11	5122	H1DAT015	6122	H2DAT015
4123	+3V	5123	H1DAT015*	6123	H2DAT015*
4124	CPMB13	5124	DGND	6124	DGND
4125	CPMB15	5125	H1DRE015*	6125	H2DRE015*
4126	–2V	5126	H1DRE015	6126	H2DRE015
4127	–2V	5127	DGND	6127	DGND
4128	DPMSLA	5128	H1LRS015*	6128	H2LRS015*
4129	DPMS1	5129	H1LRS015	6129	H2LRS015
4130	+5V	5130	DGND	6130	DGND
4131	DPMS3	5131	H1HRS015	6131	H2HRS015
4132	DPMS5	5132	H1HRS015*	6132	H2HRS015*
4133	DGND	5133	DGND	6133	DGND
4134	DPMS7	5134	ACP1	6134	ACP1 *
4135	–5V	5135	–5V	6135	–5V

Fail Log MemorY (FLMY)

Fail Log Memory (FLMY) is an optional printed circuit board for the Fusion HF tester. FLMY provides high speed capture and analysis of memory device failures. For efficient use of tester data storage, DPRO provides redundancy support, and fail masking is available.

The FLMY board is installed in the Digital Crate. One board supports 128 test channels. Two boards can be installed per Digital Crate: The Fusion HF tester can be configured with eight FLMY boards to support up to 1024 test channels for memory devices.

The FLMY boards interface to the DUT and the tester mainframe through the FARMNT boards. Standard test operations are still available when FLMY boards are installed.

Following is a summary of the functions and capabilities of FLMY:

- Generate complex test patterns (page 3-77)
- Capture data up to 250Mhz (page 3-79)
- Capture memory array configurable by device under test (DUT) width (page 3-79)
- Serial/Parallel conversion (page 3-88)
- Redundancy support (page 3-81)
- Accumulate errorspage 3-81)
- Mask errors (page 3-82)
- Log response (page 3-84)
- Address log (page 3-83)
- Analyze test results (page 3-83)
- Scope sync programmable to addresses (page 3-83)

The Data Processor Response (DPRO) features, can also be installed in the FLMY board. For information about DPRO, refer to Data Processor Response (DPRO) on page 3-84.

FARMNT Interface

Two FLMY boards can be installed in one Digital Crate to process the 256 test channels of one crate. The FLMY interfaces with the DUT through the FARMNT boards.

Depending on the number of pins per DUT, more than one DUT can be tested through each FARMNT board: One FARMNT board supports 16 test channels (pins).

Address Pattern Generator

The Algorithmic Pattern Generator (APG) is a sub-system on the FLMY board that generates complex address patterns for testing memory devices. The APG can be programmed to initiate and control the entire test of DUTs. The DUT can addressed in random order, and the same DUT address can be tested multiple times.

The sub-system consists of pattern generators, address controllers, data controllers, and memory banks.

- Control pattern memory (CPM) contains the instructions for address patterns.
- Four pattern generators (PATI) receive instructions from the CPM.
- Each PATI delivers code to an addresss controller (ADRC).
- Each ADRC controls a pair of data controllers: DATAC_0, DATAC_1.
- Each data controlloer communicates to a memory bank: MM_0, or MM_1.
- Each memory bank has an upper memory bank and a lower memory bank.
- One FLMY board can interface with 8 FARMNT boards: 128 test channels.

The APG sub-system is divided into two banks, A and B. The sub-system is shown in Figure 3.9 on page 3-78.

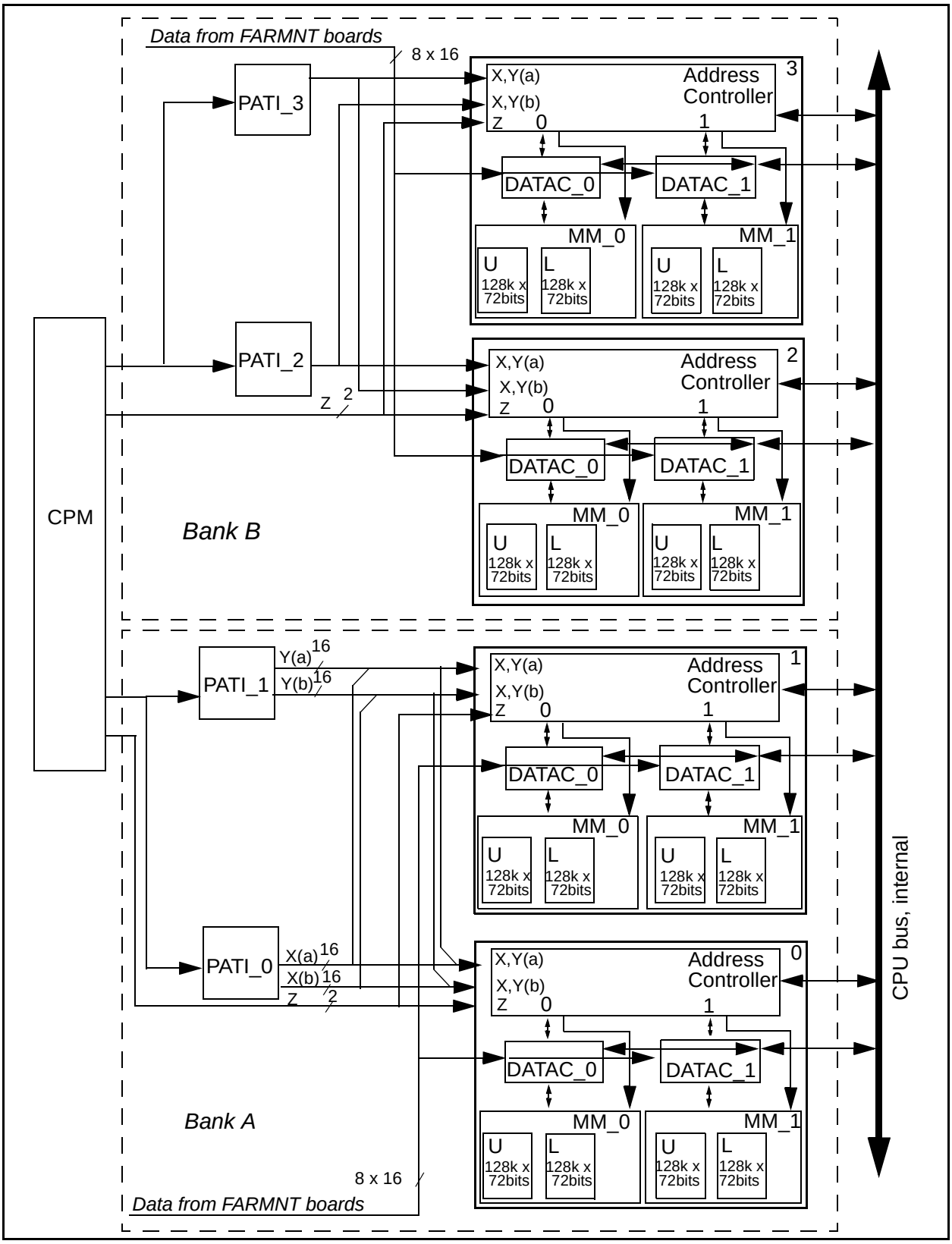


Figure 3.9: FLMY APG Subsystem

Capture Memory Configuration

FLMY has a memory array to capture DUT errors. The array can be configured to test memory devices of various widths and depths.

The configuration of the speed and depth of capture memory is determined by the test vectors (program instructions). Factors of the test vectors include the width of the DUT, the digital mode (VX125 or VX250), and bits of error response.

The maximum capture rate of the FLMY is 250Mbps. The maximum available memory varies per capture rate and bit response.

Table 3.19 lists possible configurations of speed and memory depth. The available memory shown is based on the maximum speed.

Table 3.19: FLMY Capture Array Configurations per Speed

DUT Width	Speed <= 125Mbps, 2 bits of error response (VX125 only)	125Mbps < Speed <= 250Mbps 1 bit of error response	Speed <= 125Mbps, 1 bit of error response
128 bits	n.a.	n.a.	256K x 128
64/72 bits	256K x 64/72	256K x 64/72	512K x 64/72
32/36 bits	512K x 32/36	512K x 32/36	1M x 32/36
16/18 bits	1M x 16/18	1M x 16/18	2M x 16/18
8/9 bits	2M x 8/9	2M x 8/9	4M x 8/9
4 bits	4M x 4	4M x 4	8M x 4
1 bits	16M x 1	32M x 1	32M x 1

X, Y, Z Response Bits

For the following, refer to Figure 3.9 on page 3-78.

To provide capture array addresses, the response bits of Bank A and Bank B each use their own X, Y and Z address fields.

The X and Y addresses are 16 bits each, and are provided by the PATIs. Interleaved 62.5MHz X Y addresses generate a 250MHz address stream.

There are 4 bits of Z address fields, two bits each for Bank A and Bank B. These bits are provided directly by CPM at 125MHz. Two interleaved Z bits can be interleaved to operate at 250MHz.

Response Modes

There are two response modes:

- Single-bit response
- Two-bit response

Single-bit Response Mode

In single-bit response mode the A banks represent the DUT memory lower half, and the B banks represent the upper half of the DUT. This mode doubles the capture depth.

In single-bit mode, the maximum memory width is 128 bits, and the maximum capture rate is 125MHz.

Two-bit Response Mode

In two-bit mode, the maximum memory width is 72 bits, and the maximum capture rate is 250MHz.

Serial / Parallel Conversion

To test devices with serial input/output ports, data can be converted: serial-to-parallel; parallel-to-serial.

Serial-to-Parallel

Serial-to-parallel conversion allows the Fusion HF tester to process the results of data from a serial DUT.

The instructions for serial-to-parallel conversion are provided by the CPM memory. During “de-serialization”, a single address is provided per DUT word: The address represents the resultant parallel word. After the complete word has been de-serialized, the data is written to the provided address.

The data is de-serialized by the real-time module on the DPRO board.

The number of serial DUTs that can be tested simultaneously depends on the test setup. Following are some examples:

- If the caputured data is “ping-ponged” between memory banks, a maximum of four serial DUTs can be tested per DPRO. This setup allows the DUTs to be tested at different frequencies.

- At 250MHz, up to 128 DUTs can be tested. The memory banks are shared.
- At 125MHz and one-bit response, eight DUTs can be tested if one memory bank is allocated to one DUT.

Parallel-to-Serial

Parallel-to-serial conversion allows the Fusion HF tester to deliver test patterns to a serial DUT.

The serial-to-parallel function can be configured to shift data from least significant bit to most significant bit (lsb-to-msb), or msb-to-lsb. The direction of shifting should be programmed on the order of the data out of the DUT.

Address Capture

The CPM memory provides the capture enable signal that indicates which tested addresses are valid for storage.

Redundancy Support

During pattern execution, the failures per row and column are stored during the capture of errors. The errors are accumulated without repeating the storage of the DUT addresses where failures occurred: Addresses of failures are stored as unique.

After all memory device failures have all been captured, the FLMY provides redundancy support to accelerate the analysis of the failures.

Accumulate Errors

Accumulate Errors provides a quick check of all bits that failed in the DUT.

The Accumulate Error mode logs errors multiple failures of a DUT address, without overwriting the previously logged errors that occurred at the same DUT address.

The address of the captured data is read, and the new error data is bit-wise OR'd to the already stored fail data. The result of OR is written back to that address: Each data bit that fails is recorded.

It is typical for a test program to write and then read several data patterns at the same DUT address.

Mask Errors

The memory Array data bit-wise masks the received fail data. New input errors are not recorded. Data bit errors that do not show up in the memory array — were not previously recorded, cause a fail signal to occur.

In Mask Error mode, the memory array(s) are accessed for read only, and are used to mask errors on a cycle-by-cycle basis. The mask errors are the OR'd results of the data at a single DUT address. This provides a single mask fail bit when a data bit at the DUT address fails.

In high speed mode or two-bit response mode, the A and B banks each provide a single mask fail.

Fail Log Controller

The data that Fail Log Controller logs is the DUT addresses that have failed. To not repeat data in this memory bank, the logged data is checked to see if the DUT address has already been recorded.

During a write to log memory cycle, the data controller reports if the tested address had been previously logged with a failure. If the tested address had been previously logged, then the failure data is not saved in the log memory. If no failure data had already been stored, then the data is written to log memory.

Unless masked, all fail data is stored: Sequential failures of one address are stored in a random access memory (RAM) array. An address counter, which increments for each recorded failure, including unique address failures, causes the fail data to be stored sequentially in the memory array.

Regarding unique address fails: The recorded data includes information of whether or not multiple failures occurred.

Failure Scan

Failure Scan locates failure information by searching the X and Y memory fields through X-fast and Y-fast scanning.

- X-fast scan — Increment the X address each read cycle; increment the Y address after X reaches its maximum count and restarts (rolls over).
- Y-fast scan — Increment the Y addresses each read cycle; increment X after Y rolls over.

Each recorded failure within the scan range has the following information: failed DUT address, data response at that address, and a set polling flag.

The scan function is aborted if the number of errors located through scanning exceeds the number of counted errors. The errors are counted per test channel.

Address Log

The memory depth for logged values is 1K. After 1K of addresses have been recorded, the address controller wraps around, overwriting the previously stored information. Only the last 1K of logged values is retained.

There are two modes of Address Log operation:

- Log the DUT address each test cycle
- Log only the DUT address where a failure occurs

When logging failures, specified failures can be ignored: The FLMY board receives the “ignore fail” signal from the DWBFNT board. For information on the DWBFNT board, refer to the **online manual**.

Test Analysis

The PowerPC module on the FLMY provides the control to extract and analyze the failure information in the memory array(s). This enables the FLMY to be programmed to conduct the entire test and analysis of memory devices.

Scope Sync

The ScopeSync can be triggered to X addresses and/or Y addresses. This feature supports trouble-shooting of the DUT or the test setup.

Diagnostics Support

Memory array diagnostics and other diagnostics that are appropriate are performed through the power PC module on the FLMY board. This allows faster memory diagnostics by processing all FLMY boards in parallel.

Log Response

Log response supports diagnostics. In this mode, the FLMY captures response data sequentially.

Trillium Bus Interface

Access to all registers and the memory arrays for command, control, and diagnostics of the DPRO board is through the Trillium Bus.

Data Processor Response (DPRO)

The Data Processor Response printed circuit board is an option for the Fusion HF tester. DPRO supports the test of digital signal processors (DSP), such as analog to digital (A/D) converters.

The DPRO board is installed in the Digital Crate. One board supports 128 test channels. Two boards can be installed per Digital Crate: The Fusion HF tester can be configured with eight DPRO boards to support up to 1024 test channels for DSP devices.

The signals of the DPRO boards connect to the system through the backplane of the Digital Crate.

Following is a summary of the functions and capabilities of DPRO:

- Capture data up to 250Mhz (page 3-79)
- Capture memory array configurable by device under test (DUT) width (page 3-79)
- Serial/Parallel conversion (page 3-80)
- Log response (page 3-88)
- Analyze test results (page 3-83)

Test patterns are delivered to the DSP DUTs from a source external to the DPRO board: only the data response is observed and processed. External sources include analog instruments that can be installed in the Fusion test head. For information about these instruments, refer to the online manual, *Analog Instruments*.

Fail Log Memory (FLMY), is an option that can also be available on the same printed circuit board as DPRO. For more information about FLMY, refer to Fail Log MemorY (FLMY) on page 3-76.

Capture Memory Configuration

DPRO has a memory array to capture DUT errors. The array can be configured to test memory devices of various widths and depths.

The configuration of the speed and depth of capture memory is determined by the test vectors (program instructions). Factors of the test vectors include the width of the DUT, the digital mode (VX125 or VX250), and bits of error response.

The maximum capture rate of the DPRO is 250MHz. The maximum available memory varies per capture rate and bit response.

Table 3.20 lists possible configurations of speed and memory depth The available memory shown is based on the maximum speed.

Table 3.20: DPRO Capture Array Configurations per Speed

DUT Width	Speed <= 125Mbps, 2 bits of error response (VX125 only)	125Mbps < Speed <= 250Mbps 1 bit of error response	Speed <= 125Mbps, 1 bit of error response
128 bits	n.a.	n.a.	256K x 128
64/72 bits	256K x 64/72	256K x 64/72	512K x 64/72
32/36 bits	512K x 32/36	512K x 32/36	1M x 32/36
16/18 bits	1SM x 16/18	1M x 16/18	2M x 16/18
8/9 bits	2M x 8/9	2M x 8/9	4M x 8/9
4 bits	4M x 4	4M x 4	8M x 4
1 bits	16M x 1	32M x 1	32M x 1

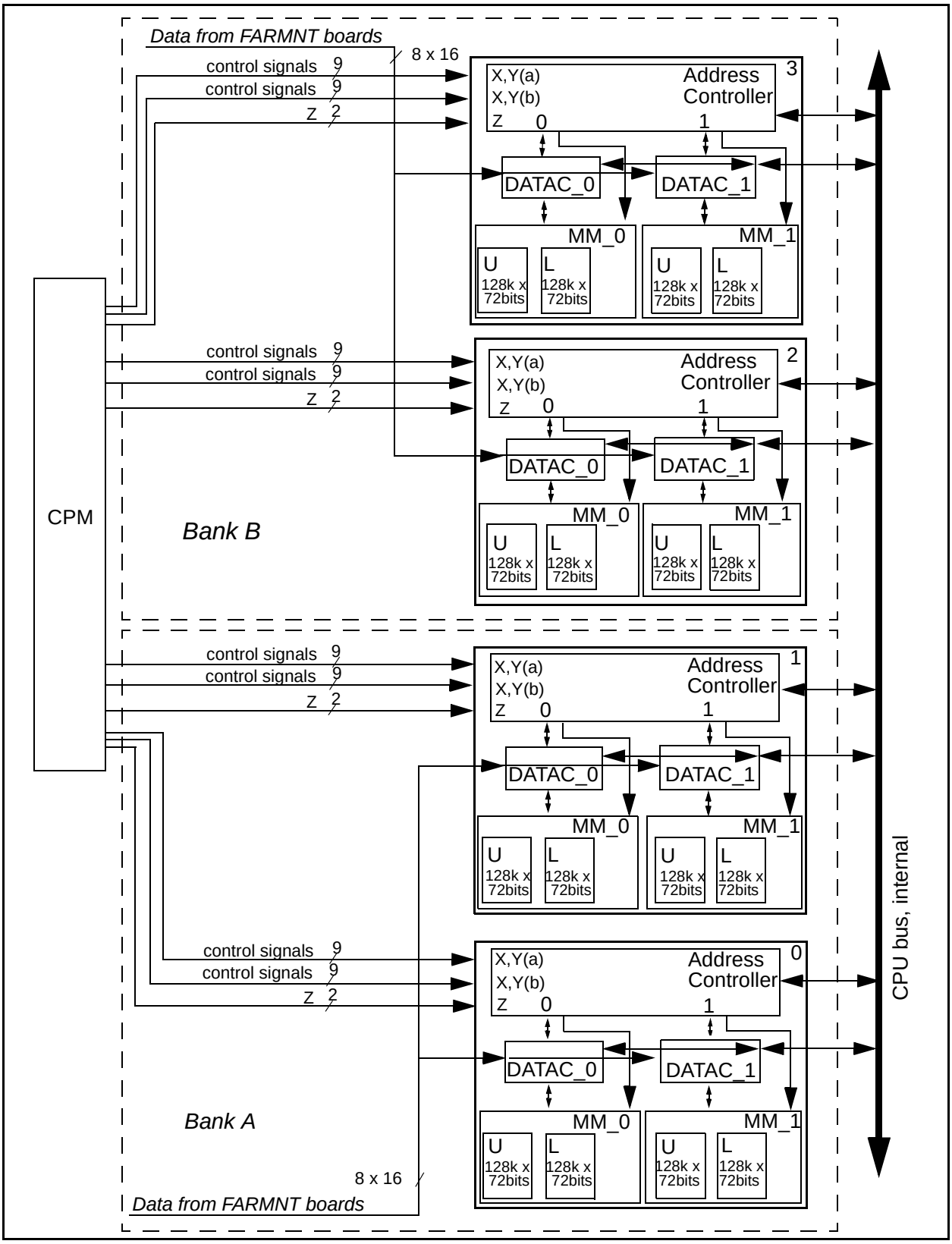


Figure 3.10: DPRO Memory Bank Subsystem

Response Modes

There are two response modes: Single-bit response; Two-bit response

Single-bit Response Mode

In single-bit response mode the A banks represent the DUT memory lower half, and the B banks represent the upper half of the DUT. This mode doubles the capture depth.

In single-bit mode, the maximum memory width is 128 bits, and the maximum capture rate is 125MHz.

Two-bit Response Mode

In two-bit mode, the maximum memory width is 72 bits, and the maximum capture rate is 250MHz.

Serial / Parallel Conversion

To test devices with serial input/output ports, data can be converted: serial-to-parallel; parallel-to-serial.

Serial-to-Parallel

Serial-to-parallel conversion allows the Fusion HF tester to process the results of data from a serial DUT.

The instructions for serial-to-parallel conversion are provided by the CPM memory. During “de-serialization”, a single address is provided per DUT word: The address represents the resultant parallel word. After the complete word has been de-serialized, the data is written to the provided address.

The data is de-serialized by the real-time module on the DPRO board.

The number of serial DUTs that can be tested simultaneously depends on the test setup. Following are some examples:

- If the caputured data is “ping-ponged” between memory banks, a maximum of four serial DUTs can be tested per DPRO. This setup allows the DUTs to be tested at different frequencies.
- At 250MHz, up to 128 DUTs can be tested. The memory banks are shared.

- At 125MHz and one-bit response, eight DUTs can be tested if one memory bank is allocated to one DUT.

Parallel-to-Serial

Parallel-to-serial conversion allows the Fusion HF tester to deliver test patterns to a serial DUT.

The serial-to-parallel function can be configured to shift data from least significant bit to most significant bit (lsb-to-msb), or msb-to-lsb. The direction of shifting should be programmed on the order of the data out of the DUT.

Test of Serial Devices

Devices with multiple output serial ports can be tested: DPRO supports testing DUTs that have 4 serial outputs each. The number of such DUTs that can be examined simultaneously depends on the test configuration.

- To test multiple serial output DUTs, they must be tested in parallel.
- At 250 MHz, a maximum of 4 DUTS can be tested.
- At 125 MHz, a maxium of 8 devices can be tested. At this frequency, the memory depth can be doubled; however, this reduces the maximum number of serial DUTs to 4.

Test of Parallel Devices

The response of DUTs of narrower width are packed into the array. The address controller of the DPRO provides the capability to store the responses.

At 250MHz, DPRO supports DSP devices of widths up to 72 bits wide. 72 bits is the standard format of the DPRO main memory array.

At 125MHz, DPRO supports up to 128 bits of width.

Log Response

The DPRO logs response data in the order received from the DUT. The response from multiple DUTs can be logged simultaneously: The DUTs are logged to separate memory banks.

When logging data at 125MHz, only one bank needs to be dedicated to one DUT.

When logging data at 250MHz, or operating the test in 2-bit response mode, two banks need to be assigned per DUT. The A and B banks respond to separate types of DUT failures.

Test Analysis

The PowerPC module on the DPRO board provides the control to extract and analyze the stored response information in the DPRO memory arrays: The DPRO can be programmed to conduct the entire test and analysis of DSP devices.

Diagnostics Support

Memory array diagnostics and other diagnostics that are appropriate are performed through the power PC module on the DPRO board. This allows faster memory diagnostics by processing all DPRO boards in parallel.

Trillium Bus Interface

Access to all registers and the memory arrays for command, control, and diagnostics of the DPRO board is through the Trillium Bus.

Waveform and Algorithmic Patterns 4

Introduction

Waveform patterns and algorithmic patterns are delivered to the device under test (DUT).

Pattern memory allows the user to program a waveform pattern for test channels. There are two devices of pattern memory: Control Pattern Memory (CPM), and Data Pattern Memory (DPM).

Algorithmic patterns support the test of memory devices. The Algorithmic Pattern Generator (APG) allows the user to deliver complex digital patterns to the DUT.

NOTE This section provides an overview of pattern memory. For detailed information about enVision++ , refer to the online manual.

Control Pattern Memory (CPM)

The Control Pattern Memory (CPM) defines all test patterns that are delivered to a device under test (DUT). CPM is located on each FARMNT board in the Digital Crate. The TSINT distributes copies of the CPM address, enable, and clock information to the DWBFNT board(s), which then delivers the signals to the FARMNT board(s).

The CPM can control the DPM and the APG.

Instruction Generator

The Instruction Generator (IGEN) is part of the pattern processor. It is interprets CPM micro instructions and generates the CPM address. It also manages flags, modes, counters, and a stack for sub routine service. The IGEN is located on the TSINT board.

CPM Instructions

CPM instructions consist of micro-instructions, conditions, and modes.

Micro-Instructions

Table 4.1 shows the micro-instructions for the CPM.

Table 4.1: CPM Micro-Instructions

Instruction	Description
NOP	Skip current vector cycle (CPM location), continue to next CPM location
COND	Select the condition to be tested with subsequent conditional operations. (applicable conditions are listed in Table 4.2 on page 4-3)
INTL	Defines location of interrupt subroutine.
LAA	Load APG address.
LDAL	Load lower value of data pattern address.
LDAU	Load upper value of data pattern address.
JMP	Jump to CPM location specified in operand
CJMP	Jump to CPM location specified in operand if selected condition is true.
JSR	Jump to CPM subroutine specified in operand.
CJSR	Jump to CPM subroutine specified in operand if selected condition is true.
RET	Return to CPM location following last JSR or CJSR instruction
CRET	Return to CPM location following last JSR or CJSR instruction if selected condition is true.
RPT value	Repeat present CPM vector number of times specified in operand (65K max)
RPTP count	Repeat present CPM vector number of times specified in operand or until pass cycle is encountered.

Table 4.1: CPM Micro-Instructions (Continued)

Instruction	Description
FLAG list	Sets or resets the flags specified in the operand.
MODE list	Sets or resets various functional operating modes.Applicable modes are listed in Table 4.3 on page 4-4
LCn count *	Load Loop Counter n (1–4) and Loop Count Register n (1–4) with 16-bit count.
DCn *	Decrement Loop Counter n (1–4). This op-code can be combined with any of the above operations in the same vector except the LCn instruction. If counter is presently at terminal count then this command reloads the loop counter from the Loop Count Register.
TSM	Modify current Time Select information.
SDP	Step (execute) data pattern.
SDPE	Step data pattern after executing RPT or SHD.
SAP	Step Algorithmic Pattern Generator.
STOP	Stop test pattern execution.
STOPF	Stop test pattern execution and set test fail status true.
TCI	Test Counter Inhibit. Enables/disables the cycle counter.
FAIL	When this mode is set, subsequent failures are ignored, including failures that would have occurred during the last np cycles.

* The LCn and DCn instructions generate algorithms through the algorithmic pattern generator (APG).

Conditions

With the micro-instruction COND, condition determines whether or not the selected instruction is executed. Conditions are listed in Table 4.2.

Table 4.2: Conditions for Micro-Instructions

Condition	Description
NZCn	Condition is true when the specified loop counter (1–4) is not zero.
FAIL	Condition is true if a functional fail was detected on the cycle that occurred np cycles earlier.
INTF	Condition is true while INTF flag is true.
APGF	Condition is true while APG flag is true. APG flag is set by APG micro-instructions.

Table 4.2: Conditions for Micro-Instructions (Continued)

Condition	Description
F1, F2, F3	General purpose flags that can be set and reset by the tester controller.
CONT	The condition is true if the CONT flag is set. The CONT flag must be set/reset either by the CPM FLAG instruction or by the tester controller.
SEQF	Condition is true if the SEQF flag is set. The SEQF flag is set by any failure that occurred prior to np cycles before testing the flag.
PLLF	Condition if true if a stable phase lock has not been achieved.
TRUE	Condition is always true. This causes all conditional instructions to become unconditional: always executed.
FALSE	Condition is always false: conditional instructions become “no-op” (are not executed).

Table 4.3 lists the mode instructions of the CPM.

Table 4.3: CPM Mode Instruction

Instruction	Description
TCI	Test Counter Inhibit: Enables/disables the cycle counter.
FAIL	When this m ode is set, subsequent failures are ignored, including failures that have occurred during the last cycles.

Data Pattern Memory (DPM)

The Data Pattern Memory (DPM) resides on the FARMNT board in the Digital Crate. The TSINT distributes the DPM start address to the FARMNT, DWBFNT, and FLMY and DPRO boards. FLMY and DPRO are optional Digital boards.

Memory Structure

The DPM consists of two 16K x 32 memories (DPACMA and DPACMB) that are accessed on alternating odd/even cycles, one vector per cycle. Each vector contains six bits of data per test channel, a period select value, and a vector repeat value.

- Period select value — Specified time interval.

- Vector — A pattern vector is a string of data that defines the waveform pattern, provides data for test comparison, defines the time interval, and specifies which test channel.
- Vector repeat value — The number of times to repeat the vector.

DPM Instruction Generator

The DPM instruction generator controls the DPM address. This address is not distributed to other boards in the system. However the control signals that generate the address are distributed to the DWBFNT, and the start address is delivered to the FARMNT.

DPM Address Generator

The DPM address generator receives instructions and data from the CPM. The DPM address is incremented by the CPM microinstruction SDP.

The start address, and its own clock and load signal, come from the instruction generator (IGEN) on the TSINT board.

Timing Generator

Each waveform memory location specifies a timing value and an "event" for each of four timing generators. The event specifies what action the timing generator is to cause at the specified timing value.

An event may be associated with the action of a driver functional strobe function, or both.

Table 4.3 shows the timing generator events.

Table 4.4: Timing Generator Events

Applicable TG's	Event	Description
All four TGs	Driver High	Switches the driver state to the "high" state. If the driver was previously in an off state, it is maintained in an off state.
All four TGs	Driver Low	Switches the driver state to the "low" state. If the driver was previously in an off state, it is maintained in an off state.

Table 4.4: Timing Generator Events (Continued)

Applicable TG's	Event	Description
All four TGs	Drive On/ High	Switches the driver state to the "high" state. If the driver was off, than the driver is turned on concurrent with switching to the high state. (see note 1)
All four TGs	Drive On/Low	Switches the driver state to the "low" state. If the driver was off, than the driver is turned on concurrently with switching to the low state.(see note 1)
All four TGs	No Event	Timing Generator is disabled in this waveform. No timing value is applicable.
All four TGs	Driver On	Switches the driver on state and to the last level state set by one of the above events.
All four TGs	Driver Off	Switches the driver off
TG3 & TG4	Edge Strobe - High	Strobes the comparator data for a valid "high" state
TG3 & TG4	Edge Strobe - Low	Strobes the comparator data for a valid "low" state
TG3 & TG4	Edge Strobe - Float	Strobes the comparator data for a valid "float" state. (> CVL reference and < CVH reference)
TG3 & TG4	Open Window Strobe - High	Opens a window strobe which will compare for a valid "high" state until closed.
TG3 & TG4	Open Window Strobe - Low	Opens a window strobe which will compare for a valid "low" state until closed.
TG3 & TG4	Open Window Strobe - Float	Opens a window strobe which will compare for a valid "float" state until closed. (> CVL reference and < CVH reference)
TG3 & TG4	Open Window Strobe - Not Float	Opens a window strobe which will compare for a valid "not float" state until closed. (< CVL reference or > CVH reference)
TG3 & TG4	Close Window Strobe	Closes any window strobe that has been previously opened by any of the Open Window Strobe events.

Algorithm Pattern Generator (APG)

The Algorithm Pattern Generator (APG) provides algorithmic test patterns for each test channel. AGP supports testing memory devices, as it allows memory addresses to be tested in non-linear order (pseudo-random, butterfly pattern, etc.). This feature is essential when the optional Digital Crate board, Fail Log Memory (FLMY), is installed.

The APG functions in both VX125 and VX250 digital modes.

APG Instructions

The microinstructions for the APG are stored in the Control Pattern Memory (CPM). The APG is controlled by the CPM.

When the APG is running in the VX125 digital mode, six address bits are available for selecting sixty-four instructions.

When APG operates in the VX250 digital mode, the CPM is limited to three address bits: eight instructions. The number of available instructions can be increased by appending instructions to specified digital modes: The test program can be written to use both VX125 and VX250 modes. To alternate between VX125 and VX250, the mode must be selected before the instruction is executed.

For information about the VX125 and VX250 digital modes, refer to Digital Modes on page 1-3.

For detailed information about enVision++ software, refer to the online manual.

Table 4.5 lists the micro-instructions for APG.

Table 4.5: Algorithm Pattern Generator Micro-Instructions

Instruction	Mode	Description
LOAD	All	Loads an initial field value into the Foreground Register.
NOP	All	No operation to any of the registers.
INC	Address	Increments the Foreground Register.
DEC	Address	Decrements the Foreground Register.
LSH0	Shift Left	Shifts the Foreground register left and fills in a “0” into the least significant bit.

Table 4.5: Algorithm Pattern Generator Micro-Instructions (Continued)

Instruction	Mode	Description
LSH1	Shift Left	Shifts the Foreground register left and fills in a “1” into the least significant bit.
RSH0	Shift Left	Shifts the Foreground register right and fills in a “0” into the most significant bit.
RSH1	Shift Left	Shifts the Foreground register left and fills in a “1” into the most significant bit.
LROT	Rotate	Shifts the Foreground register left while shifting the most significant bit into the least significant bit.
RROT	Rotate	Shifts the Foreground register right while shifting the least significant bit into the most significant bit.
PUT	All modes	Loads the present Foreground Register value into the Background Register.
SWAP	All modes	Swaps the contents of the Foreground and Background registers.
INV	All modes	Selects the Inverse of the Foreground register as the pin data source on the present vector.
BGD	Normal	Selects the Background Register as the pin data source on the present vector.
AND	AND	Selects the Background Register AND’ed with the Foreground Register as the pin data source on the present vector.
OR	OR	Selects the Background Register OR’ed with the Foreground Register as the pin data source on this vector.

Low Speed Digital 5

Introduction

The low speed operation of digital test is the initial setup of the test conditions, the processing of test results, and reading status registers.

Functional Overview

A test channel provides the means to generate and deliver programmed test parameters to one tester pin, which can be connected to one DUT pin, and to evaluate and record the response of the DUT pin. A summary of the test process follows.

- To set up the test conditions, the programmed vectors are downloaded and decompressed.
- The appropriate instructions are then delivered to the appropriate tester channels: Each tester channel receives its own set of instructions.
- These instructions include the test patterns (waveforms) to deliver to the DUT, the DUT signals to receive and evaluate, which results to save to memory, and the maximum number of results to save.

In the Digital Crate, to ensure the necessary signals are synchronized, clocks on different boards are referenced to the same source clock: REFCLK on the master Timing Sequencer Instruction Generator (TSINT).

If a Pin Electronics Card (PEC) error occurs, an interrupt signal is generated. Potential errors are excess temperature of the PEC, or overloading from a DUT.

Hardware Overview

To perform low speed functions, the appropriate boards interact and carry out specific tasks. Refer to Figure 5.1, Digital Subsystem, low speed, on page 5-5 for the routing of the functions of low speed Digital.

NOTE Figure 5.1 is not a complete diagram of the Fusion tester; it is a reference for low speed operation.

Bus Interface

A bus interface is a transmission path through which various boards communicate: signals are delivered and received. Each board has a unique address, which enables a board to recognize the signals that are delivered to it.

TPAT2A Board

The Test Program Accelerator Trillium (TPAT2A) decompresses the test program, and writes test patterns. The TPAT2A also provides the initial stage of communication between the tester mainframe and the test head. TPAT2A supports 1024 tester channels.

TLBD Board

The Turbo Load Board (TLBD) interfaces the tester mainframe to the test head through the serial bus. To send data, parallel words are reformatted to serial streams, then transmitted across the bus. Received serial data is formatted to parallel words, then distributed.

CBIFNT Board

The Computer Bus Interface (CBIFNT) interfaces the TPAT2A to the boards in the Digital Crate.

VME Crate

The VME Crate contains the computer system of the Fusion tester. In low speed Digital test operation, the primary responsibilities of the VME boards are to interface with the Fusion HF test head and the Digital Crate, and to to decompress the test program.

Tester Mainframe Test Channels

This section describes the functions of the Fusion HF mainframe boards during test execution.

FARMNT Board

Each Format Response Memory (FARMNT) board supports 16 tester channels. When fully configured, there are 16 FARMNTs per Digital Crate. These boards contain the CPM and DPM memory banks, which store the patterns and the timing of the test signals that are delivered to the DUT. There are one CPM and one DPM per test channel.

DWBFNT Board

One DWBFNT functions with 128 tester channels. One DWBFNT interfaces eight FARMNT boards to the TSINT. To support the 256 tester channels per Digital Crate, there are two DWBFs per Digital Crate. The primary function of the DWBFNT is to buffer signals: TSINT signals are buffered and sent to the FARMNTs; FARMNT signals are buffered and delivered to the TSINT.

TSINT Board

The Timing Sequencer Instruction Generator (TSINT) is the digital control board, and supports 256 tester channels. TSINT stores and executes microinstructions, and distributes the reference clock (REFCLK) to the Digital Crates. There is one TSINT per Digital Crate.

Digital Crate

Each Digital Crate, when fully configured, supports 256 tester channels. The boards in the crate set up and execute test commands.

Test Head Test Channels

During low speed operations, the test head communicates to the tester mainframe through the G-Link serial bus. The DC levels of the test signals are set in the PECHFs, and the status of the PECHF registers is read by the tester mainframe.

THBDHF Board, THBUF Modules

The Test Head Bus Driver (THBDHF), accompanied with four Test Head Buffer boards (THBUF), interfaces the Fusion test head to the Fusion mainframe through the serial bus. Each THBUF module supports 256 tester channels.

Per test head, there are one THBDHF and four THBUFs.

PECHF Board

During low speed operation, The PECHF boards receive and set the values of voltage and current for drivers, comparators, loads, and clamps.

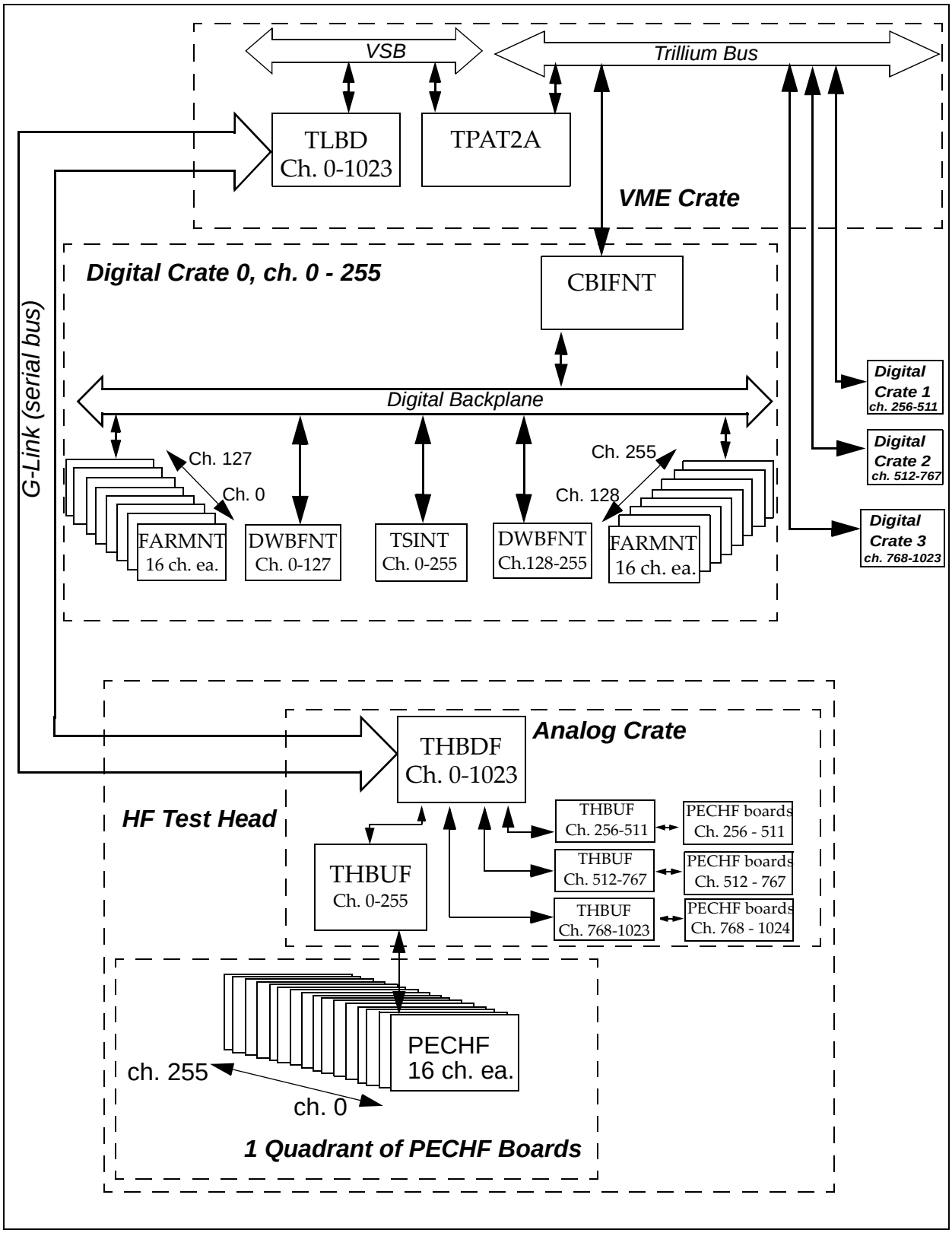


Figure 5.1: Digital Subsystem, low speed

Pattern Memory Loading

Test patterns, logical waveforms, are stored in memory: control pattern memory (CPM) and data pattern memory (DPM). They each deliver data bits that control the functions of the PECHF pin channels.

One CPM and one DPM functions per tester channel. These vector memory banks are located on the FARMNT boards. During high speed operation, commands from the CPMs and the DPMs are sent directly to the PECHFs.

For detailed information about the PECHF board, refer to th eonline manual *Test Heads and Interface Boards*.

CPM

A CPM provides 16k x 32 of vector memory, which are presented as 8 bits wide per tester channel: 2 bits are pattern source select, 6 bits are vector data. A CPM also delivers instructions for the tester channels, and the start address and step instructions (SDP, increment of the address) for the DPM.

A CPM can use a large set of microinstructions. Test patterns that can be constructed of various sub-patterns, which are executed in specified orders, are placed in the CPM. CPM supports instructions to jump to a specific address, return to the last address, perform the following instruction during a specific condition, and others.

DPM

A DPM provides 16Mbits of memory per tester channel, which can be configured as 512k x 16 x 2, or as 1M x 8 x 2: 6 bits of DPM vector memory per tester channel. DPM only responds to basic commands such as step (advance), and repeat. Test patterns of greater length that are constructed of simply repeatable sub-patterns are placed into DPM.

Voltage and Current Levels

In low speed operation, voltage levels are set on the PECHFs for drivers, comparators, programmable loads, and clamps. Current levels are set for programmable loads.

Digital values are delivered to data-to-analog converters (DAC), which then generate the desired voltage levels. These levels are set as programmed: individually, per tester channel. All PECHF DACs have 13 bits of resolution.

NOTE Additional information regarding PECHF drivers, comparators, and programmable loads is available in the Online Manual, *Test Head and Boards, HF Test Head*.

Driver

The driver delivers the test pattern to the DUT through a tester pin. To deliver the two voltage levels, digital high and digital low, the driver has two voltage references: DVH, and DVL. During high speed test execution, the driver receives the appropriate voltage level to deliver: It is more efficient to switch between two fixed voltage references, than to reset the value of the DAC and wait for the output voltage to settle.

There is one driver per tester channel.

Comparators

The comparators receive the response from the DUT, then compare the response to the expected voltage level. To effectively respond to two voltage levels, digital high and digital low, there are two comparators, COMP_HI and COMP_LO. One DAC, CVH, delivers the programmed reference voltage to COMP_HI. Another DAC, CVL, provides the reference voltage for COMP_LO.

There is one pair of comparators per tester channel.

Programmable Load

Each tester channel has two programmable current loads: source, which delivers current to the DUT, and sink, which draws current from the DUT. The direction of the current is set by the voltage reference (VREF), which is generated by a DAC: To maintain balance on a bridge network, with VREF set on one side, the DUT generates an equivalent on the other side of the bridge network.

The level of source current is determined by setting the DAC that generates ISNK. ISRC, the programmed level of source current, is delivered by a separate DAC.

Clamps

The purpose of clamps is to resolve any impedance mismatch between the DUT and the tester channel, and to protect the PECHF from damage. There are two clamps per channel: one high clamp, and one low clamp.

Impedance mismatch is a potential problem when the output of the DUT is significantly different from the impedance of the tester pin: The voltage levels of exchanged signals are likely to ring: generate excess voltage swings. To prevent this problem, the clamps are programmed to specified levels: Transmission Clamp High (TCH), and Transmission Clamp Low (TCL).

If a DUT fails, there is the possibility of excessive current forced onto the PECHF. If a clamp detects excess current, all relays in the affected tester channel are opened, and an interrupt signal is delivered to the tester mainframe through the serial bus (G-Link). The level of maximum current is fixed at 25mA. Excess current is detected through Zener diodes.

Pin Mode Selection

Pin mode selection is the operation of functions in the PECHF: high/low signal, on/off driver, and on/off load. In high speed operation, test execution, these functions are controlled by two signals from the timing generator: I/O, and Data. In low speed mode, the test program determines how the control signals are used: Either the I/O and data signals are used separately, or they are exclusive or'd.

Synchronization Clock

During high speed operation, test execution, it is necessary that the timing of the signals is synchronized. Signals can be either referenced directly to an external frequency source, or to an internal frequency source. The source is selected by the TSINT.

Single Clock Source

In the Digital Subsystem, all boards in the Digital Crates are synchronized to the same reference clock (REFCLK). REFCLK is distributed from the master TSINT, the TSINT that resides in Digital

Crate 0. The master TSINT regenerates the REFCLK from the reference frequency that is supplied by the Programmable Time Source (PTS) unit.

Alternatively, each TSINT can be set to use its own reference clock: Each TSINT contains a voltage crystal oscillator (VCO) module that is phase-locked to the REFCLK, which is distributed by the master TSINT.

NOTE The use of individual reference clocks for TSINTs is typically for diagnostic purposes only.

High Speed Digital 6

Introduction

The high speed operation of digital test is the delivery of programmed test signals to the DUT, the comparison of the DUT response to the expected response, and logging test data.

Functional Overview

During test execution, pass/fail comparisons are generated by the Pin Electronic Cards HF (PECHF) in the test head. These results are stored in the test head until the tester mainframe collects the data.

- The test patterns stored in CPM and DPM are initiated by delivering the start address to the pattern memories.
- The patterns are delivered from the FARMNTs to the PECHFs through the high speed cables. One FARMNT is connected to one PECHF, each of which supports 16 tester channels.
- For each tester channel, a PECHF executes the test patterns, and compares the response of the DUT per selected test (clock) cycle. If instructed to do so, a FARMNT measures the frequency of the data from the PECHF.
- The comparisons are returned to the FARMNTs via high speed cables. The selected comparisons are evaluated as pass/fail: the fails are logged. For the TSINT to process the data correctly, the data is synchronized for logging.

Hardware Overview

To perform high speed functions, the appropriate boards interact and carry out specific tasks. Between the test head and the tester mainframe, data is transferred through high speed parallel cables that connect the FARMNTs to the PECHFs.

Refer to Figure 6.1, Digital Subsystem, high speed, on page 6-5 for the routing of the functions of high speed operation.

NOTE Figure 6.1 is not a complete diagram of the Fusion tester; it is a reference for the high speed operation of digital test.

VME Crate

The boards in the VME crate receive and process the logged data.

Digital Crate

The boards in the Digital Crate execute test commands and process test results.

A summary of the Digital Crate printed circuit boards follows. For additional information, refer to Digital Crate on page 3-1.

TSINT Board

In high speed operation, the TSINT executes microinstructions and logs test data. The TSINT provides the period starts, controls the start up and shut down, controls the sequencing, and generates CPM and DPM addresses for the pattern sequence.

A TSINT also logs the fail count (number of failures). If programmed to do so, the TSINT ignores selected failures.

DWBFNT Board

The primary function of the DWBFNT is buffering signals between the TSINT and the FARMNTs: Control and address signals are transferred from the TSINT to the FARMNTs; fail (test) information from the FARMNTs is buffered to the TSINT.

The fail signals from the supported FARMNTs are OR'd together: Per test cycle, if one or more fail signals is received, one fail signal is delivered to the TSINT. The DWBFNT also provides a fail clock (CFPS, a delayed PSCLK) to the FARMNTs.

To support the test of multiple DUTs, DWBFNT provides a log to store the count at which a fail occurred, and from which FARMNT the fail was reported. Indirectly, this information specifies which PECHF received the DUT error, as each FARMNT is dedicated to a specific PECHF.

FARMNT Board

In high speed operation, the FARMNTs interact directly with the test head PECHFs through high speed cables. The FARMNTs provide the Drive and I/O signals to the PECHFs, and strobes the compare signals from the PECHFs. The timing of the strobes is based on user-programmed pattern and timing.Compare results are forwarded to the DWBFNT, and then to the TSINT.

Each FARMNT has one CPM and one DPM, which are the sources of data for the PECHFs to deliver test signals, and to evaluate (pass/fail) the response of the DUT.

Test Head

During test execution, almost all activity takes place in the PECHFs; the THBDHF only processes interrupts: The serial bus is too slow to process high speed data.

PECHF Board

During high speed operation, the PECHFs deliver signals to the tester pins as specified by test vectors: waveforms, voltage levels, current levels. The PECHFs also compare the responses of the DUT pins to the expected results: The PECHFs can be programmed to ignore specific DUT responses. The comparisons are delivered to the tester mainframe FARMNTs for processing. To allow sufficient time for all data to be collected and processed by the tester mainframe, the delivery of comparisons is delayed via registers.

The timing of the execution of test processes (driver output high/low, driver on/off, current load, comparison,) are controlled by timing edges. Each FARM also delivers four timing events to a PECHF per tester channel: TG1, TG2, TG3, TG4.

THBDHF Board, THBUF Modules

During test execution, the serial port is used only to transfer interrupts. The PECHF tester channel setups that were carried out during low speed operation do not change during high speed operation.

For more information, refer to the online manual *Test Heads and Interface Boards*.

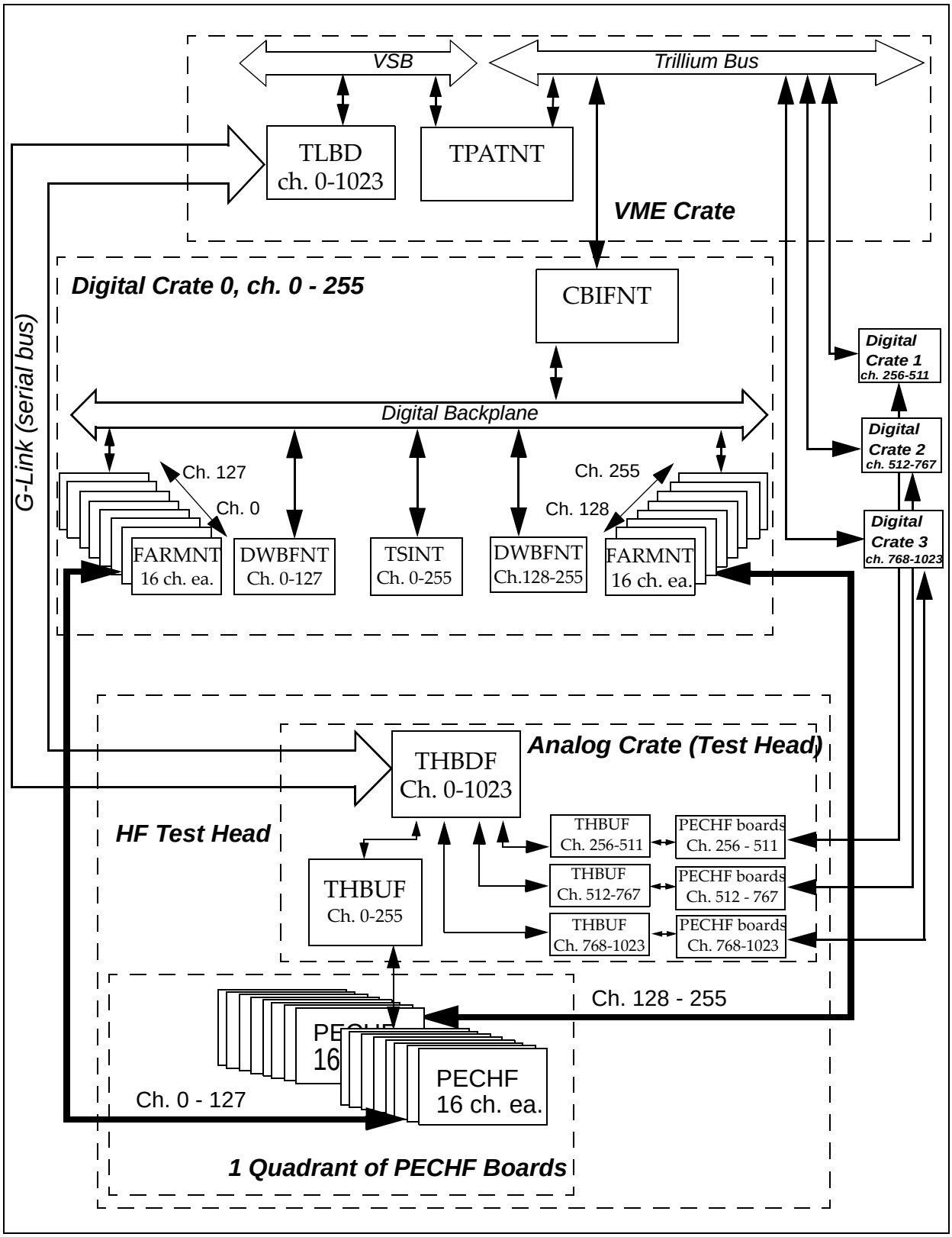


Figure 6.1: Digital Subsystem, high speed

Test Pattern Timing Control

During high speed operation, the test patterns stored in CPM and DPM are executed. The test process can include looping (repeating) a series of instructions, skipping a set of instructions, ignoring specific fails, stopping the test after all test patterns have been executed, and stopping the test if a specified number of DUT fails are logged.

For addtional information about test patterns, CPM and DPM, refer to Waveform and Algorithmic Patterns on page 4-1

Sequence Control Logic

The Sequence Control Logic controls the process of starting and stopping the operation of the test pattern.

Start Address

To start the test, the TSINT generates the CPM start address (CPMA), the DPM start address (DPMA), and the Local Time Set Memory (LTSA), all of which are delivered to the FARMNTs through the DWBFNT.

CPM

Although the memory bank of CPM is significantly smaller than that of the DPM, the CPM can process complicated test patterns. During test execution, all control signals and the CPM address are received by the FARMNT from the DWBFNT.

CPM Memory

The CPM vector memory is 16k by 8 bits. Six bits are data bits per tester channel, two bits control the pattern source selection.

CPM Instruction Memory

The CPM Instruction memory contains the CPM microinstructions, the CPM branch address, the CPM repeat count, and the CPM mode bits.

CPM Instruction Generator

Based on the contents of CPM instruction memory, the CPM instruction generator controls the CPM address (CPMA). Address, Count, Count Plus Address.

Instructions to stop, trigger, and ignore fail can be controlled by the current address, or the count, or both the address and the count.

The instructions are listed in CPM Instructions on page 4-2.

Stop on Address

The current CPM address (CPMA) is compared to the stored address. When the CPMA matches the stored address, the test pattern stops.

Stop on Count

A test counter is set to the number of vector cycles. For each cycle, the tester counter decrements. When the counter reaches zero, the test pattern stops. Stop on count can be used for both straight line vectors and looping vectors.

Stop on Address and Count

When the current CPMA matches the stored address, the counter is activated. When the counter decrements to zero, the test pattern stops.

The operation of the other processes (loop, trigger, ignore on fail) are similar to the above.

DPM

The TSINT distributes the DPM start address directly to the FARMNTs. The DPM control instructions are sent to the DWBFNTs, which are buffered and delivered to the FARMNTs. The DPM start address is accompanied with a clock and load signal.

The DPM vector memory can be configured as 16M by 6 bits, 8M x 6 bits, 4M x 6 bits, or 2M x 6 bits.

DPM Control Memory

The DPM control memory consists of two 16K x 32 bit CMOS memories (DPACMA and DPACMB) that are accessed on alternating odd/even cycles, one vector per cycle.

DPM Instruction Memory

The DPM instruction generator controls the DPM address based on the Load DPM Address (LDA) instruction, the Step Data Pattern (SDP) instruction and the DPM repeat count.

Frequency Counter

The TSINT has a frequency counter that can check the frequency of the signal from a tester pin channel. Only the master TSINT is configured to measure the frequency.

Failure Log

The high speed input to the TSINT consists of fail signals from the two DWBFNTs, which receive and combine the fails fro the FARMNTs that the DWBFNT supports. There is also a set of signals used to provide interlock of the TSINTs when multiple Digital Crates are slaved to the master.

To support the test of multiple DUTs, DWBFNT provides a log to store the count at which a fail occurred, and from which FARMNT the fail was reported. Indirectly, this information specifies which PECHF received the DUT error, as each FARMNT is dedicated to a specific PECHF.

Pattern/Response Log

The FARMNT records the fail information, received from the PECHF in a pattern/response log. Two modes of logging are available:

- Record two bits of fail data and two bits of pattern data per tester channel.
- Record the compare results from a pair of tester tester channels.

Mask

Fail data that is masked is not logged (when the test conditions meet the settings of the mask). The TSINT supports two types of masking: low speed, high speed.

Fail Mask, Low Speed

In the entire group of tester channels in the selected DWBFNT-supported group (128 channels), all individual fail bits are blocked from the TSINT: The fails are not logged, which prevents the TSINT from responding to the fails (matching or branching logic, or distribution of fail data to other TSINTs in the tester mainframe).

Fail Mask, High Speed

The high speed Fail Mask does not block fails to the slave TSINTs, and does not interfere with the branch on fail capability on the TSINT. Only the master TSINT is blocked from stopping patterns on fails: The fails are still logged in the status register.

The high speed fail masking is provided by two sources: a CPM instruction; mask by count and/or address (performed by the TSINT).

Mask by Count

A test counter is set to the programmed count, and decrements on each vector cycle. Until the test counter counts down to zero, fails are masked.

Mask by Address

The CPMA is compared to the stored ignore fail address. Fails are ignored until that address is executed.

Mask by Address and Count

The ignore fail on address plus count mode is provided by combining the ignore fail on address mode with the ignore fail on count mode. In this mode, when the address compare is true, the ignore fail on count test counter is started instead of clearing the ignore fail signal.

Log Fails Only

In the mode of Log Fails Only, the address logs for CPMA, DPMA, and LTSA, the Period Accumulate Log and the Fail Quad log only record data when a fail is detected. The purpose is to track the pattern and response log memories on the FARMNT.

Fail Counter

TSINT controls the Fail Counter. The Fail Counter tracks the number of cycles in which a fail has occurred. This enables the TSINT to execute pattern shutdown after the specified number of fails. The counter counts down from a stored value each time that the Fail Count Pointer is incremented. When the Fail Counter decrements to zero, a stop signal is sent to the Sequence Control Logic.

Stop Test

When the test concludes, TSINT stops the sequence control logic. The test terminates at the end of the test program, or when the fail counter reports the specified maximum count of failures has occurred.

Three stop modes are available: stop on address, stop on count, stop on address plus count.

Stop on Address

Stop on address is provided by comparing a stored stop address with the CPMA on each cycle. When they match a stop signal is sent to the sequence control logic.

Stop on Count

Stop on count is provided by a test counter that counts down from a stored stop value. When the counter reaches zero the stop signal is sent to the sequence control logic. The stop counter is reloaded by INIT at the start of each pattern execution. The counter normally does not count when the test count inhibit (TCI) signal is true. However, there is a mode bit that will allow it to count when TCI is true.

Stop on Address and Count

The stop on address plus count mode is provided by combining the stop on address mode with the stop on count mode. In this mode when the address compare is true the stop on count test counter is started instead of sending the stop signal to the sequence control logic. The pattern then stops normally when the test counter reaches zero

Synchronize Stop On Fail

To synchronize the test pattern to stop on fail, an OR'd version of the six fails that each TSINT receives is delivered to the master TSINT. The resultant single fail bit is cyclically aligned to the fail bits on the master TSINT before issuing the stop command to all TSINTs.

Test Counter

The TSINT contains two test counters in the Test Count Field Programmable Gate Array (FPGA). Test Counter A counts all cycles of the test pattern. Test counter B counts all cycles in which test count inhibit, a CPM instruction, is false.

When a test pattern stops running, both test counters report the correct count.

Test Channel Architecture

Tester channels are separate paths to and from the DUT. Other than synchronization, each tester channel functions separately: Each tester pin delivers a specified test pattern to the DUT, and the signal received from the DUT is evaluated by the tester as programmed.

Test patterns that are stored in pattern memory are delivered to the components that interact with the DUT.

Delivery of Test Signal to Device Under Test (DUT)

The PECHF boards transmit the test waveforms, and receive DUT response through the System Configuration Module, the Split Interface Plate, and the user-defined DUT Interface Board. (For detailed information about these interface modules, refer to the Online Manual, *Test Heads and Interface Boards.)*

I/O Mode Control (Formatter)

The I/O mode control is also known as a formatter. I/O mode control controls the output of the driver, the current load, and the comparators. On the PECHFs, each tester channel circuit has I/O mode control.

Driver

The driver generates the signal that is delivered to the DUT. The waveform is based on programmed drive levels, the hi/lo control signal, and the enable control signal.

- The programmed drive levels are the voltage levels of logic high and logic low. These voltage levels are generated by Digital-to-Analog Converters (DACs). The digital word that sets the DAC is stored in a register. During the test, the voltage levels of the logic values are not changed: The timing of resetting the output of the DAC does not support digital test.

- The hi/lo control determines whether the delivered signal is logic high or logic low. The command of hi/lo control is delivered from either the CPM or the DPM, through I/O mode control, to the driver.

- The enable control signal determines whether or not the driver is active. When the driver is not active, it is in a state of high impedance. This function supports the test of bidirectional ports. Enable control is delivered from either the CPM or the DPM, through I/O mode control, to the driver.

Drivers are located on the PECHF. One driver is available for each tester channel.

Current Loads

The I/O mode enables and disables the current load bridge circuit.

Measurement

The digital response of a DUT is measured with two comparators: The output of a DUT is compared to the expected results that were specified by the test program. The factors of the comparisons include timing, voltage level, current level, and logic value.

The results of the comparator, high or low, are delivered to the tester mainframe for processing. The test program specifies, per test cycle, if high or low indicates fail.