Fusion HF Test Head

2

Introduction

The Fusion HF test head is a mixed signal test head for the Fusion HF tester. This test head provides 1024 high-performance digital pins and 1024 ground pins, 512 general purpose pins, and 16 connections for RF signals to the device under test (DUT).

Two HF test heads can be connected to one Fusion HF tester. Running tests simultaneously is not supported. However, their functions can be alternated: While one test head exercises the DUT, the other test head bins (sorts) the device it tested.

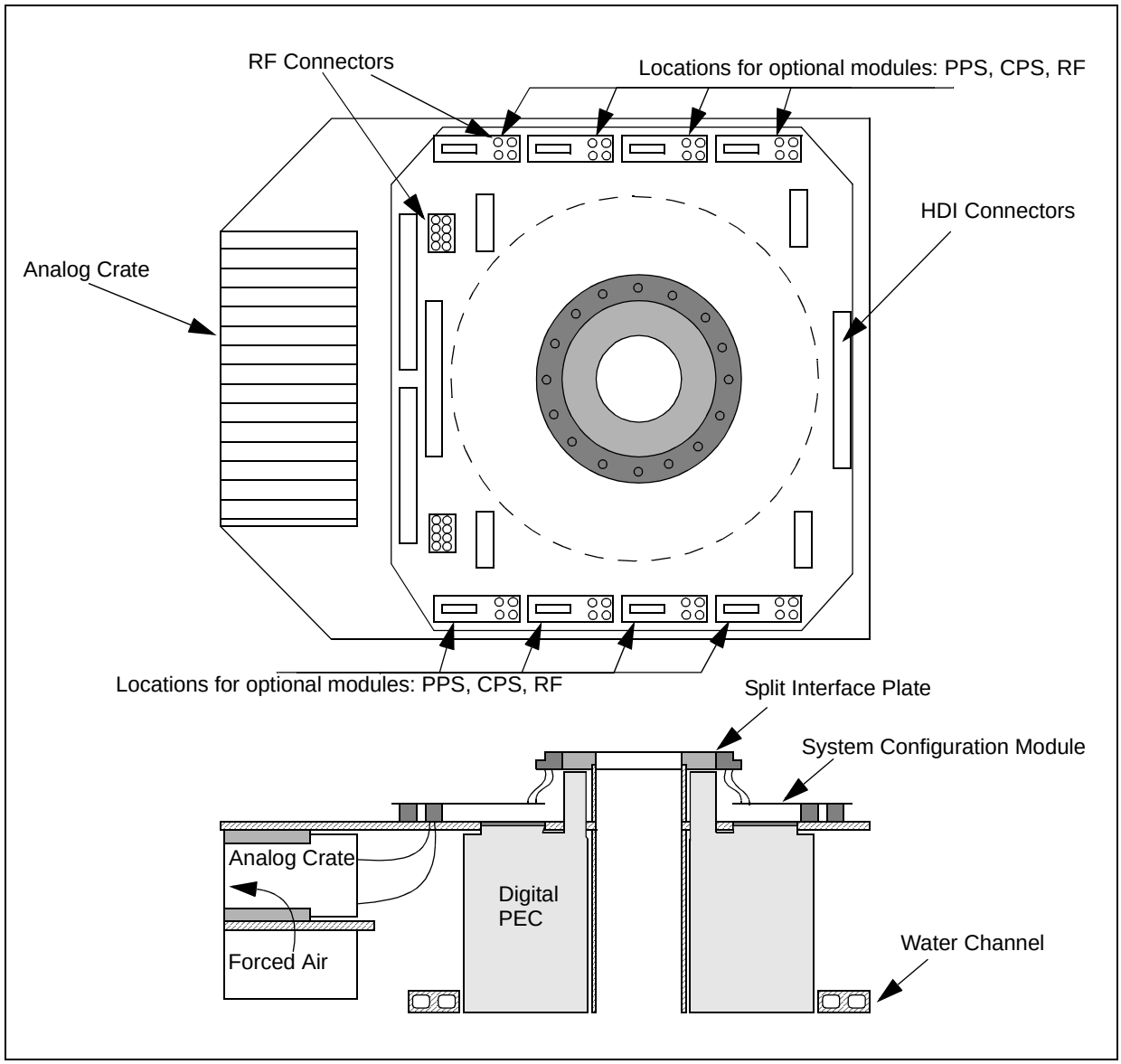

Figure 2.1: Fusion HF Test Head

Test Head Boards

The test head boards connect the device under test (DUT) to the tester mainframe. In addition to the mechanical interface, there is an electronic interface to power the DUT, deliver test signals, and receive and evaluate the response from the DUT.

Split Ring Interface Plate

The Split Interface Plate is divided into two sections with spring pins: An inner plate with 1024 digital pins and 1024 ground pins; an outer plate with 512 general purpose (GP) pins; slots for 16 RF cables. The GP pins allow for additional connections to the DUT: Either signals to/from the Digital System Configuration Module (DSCM), or user-defined input/output signals.

The DUT Interface Board (DIB, also known as load board), connects to the Split Interface Plate through spring pins to establish electrical connections to the Fusion HF test channels. The vacuum pulldown, and the spring pins (that have internal springs) apply pressure to contact the DIB.

The layout of the spring pins is divided into four sections. There are open areas, 90 degrees apart, that allow vacuum sealed socket mounting hardware.

Signal Layout. The digital signals from Pin electronics cards (PECHF) connect directly to the center plate of the Split Interface Plate. Analog signals, and user-defined signals, can be connected to the outer ring of the Split Interface Plate. The outer ring also has openings where RF cables can be placed to connect to the underside of the DIB.

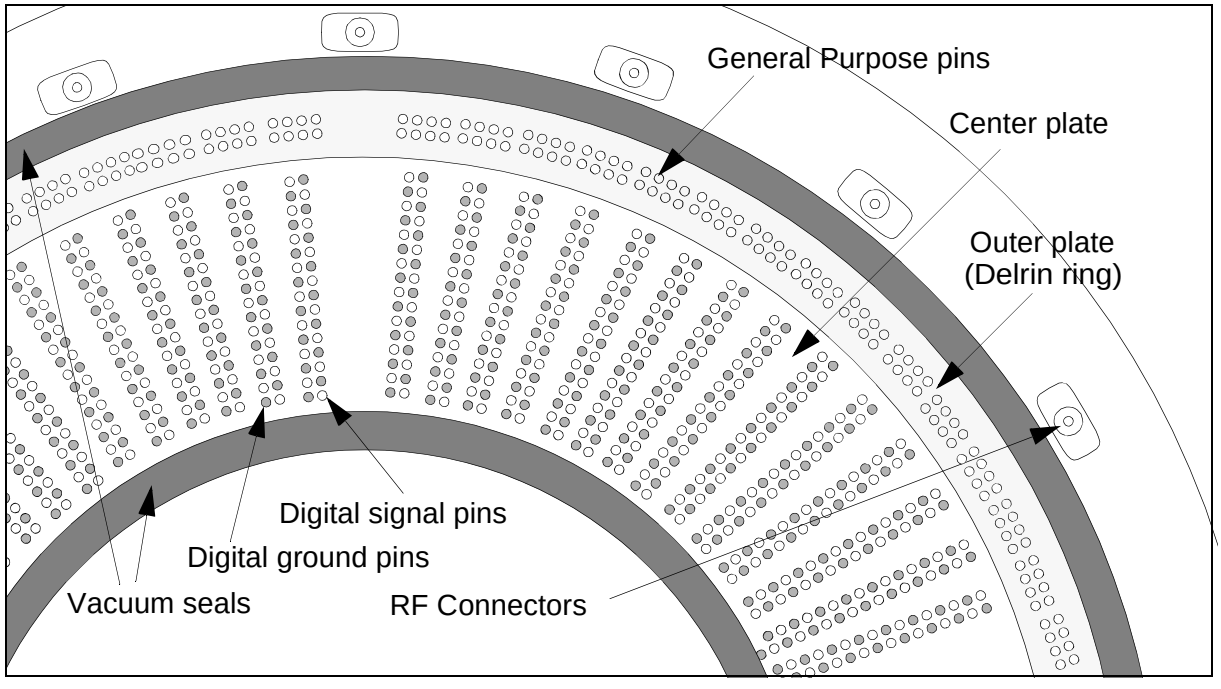

Figure 2.2: Split Interface Plate, Top View

Digital Pin Interconnect. The center plate of the Split Interface Plate provides 1024 digital pins and 1024 ground pins. The pins are distributed in 64 groups of 16 pairs of pins. This layout corresponds to the board placement and the pin layout of the PECHFs.

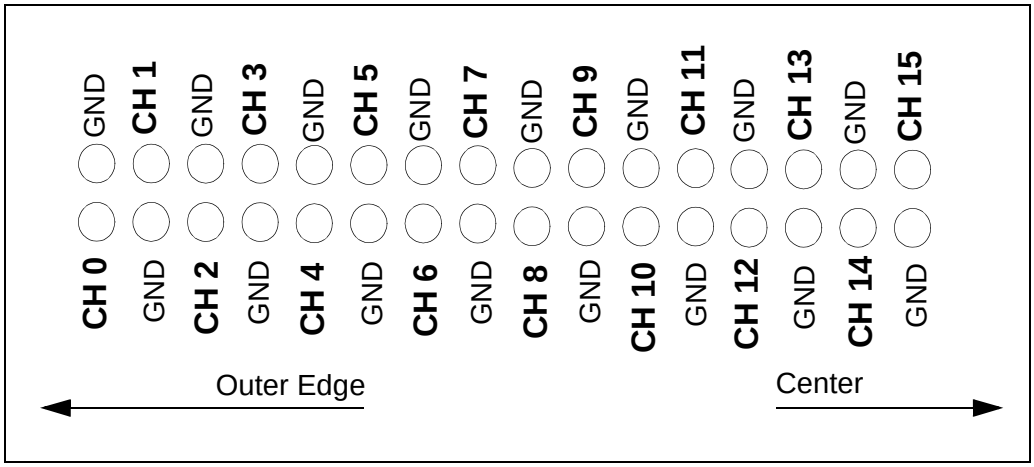

Figure 2.3: High Speed Digital Pins Center Plate, Top View

On the bottom-side of the center ring, there are 25 mil square posts that are extensions of the spring pins. These square posts provide connectors to the PEC boards. The Fusion PECHF boards have coaxial cables, which are supported by a metal frame, that directly connect high-speed digital test channels to the interface plate.

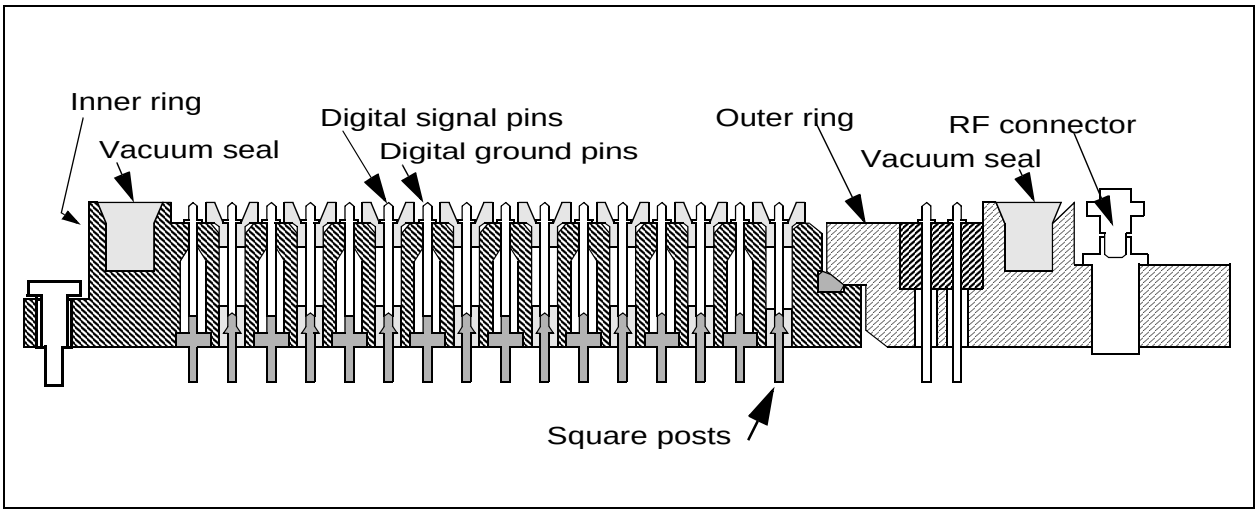

Figure 2.4: High Speed Digital Pins on Center Plate, Top View

General Purpose Pins. The outer plate has 64 groups of 8 spring pins. On the bottom-side of the plate, these pins are extended to 8-pin connectors.

The GP spring pins can be connected to the DSCM by mating the connectors with cables. These signal connections can be either default or user-modified. For more information, refer to Default DSCM Signal Connections on page 2-8

RF Signals. On the outer plate there are 16 openings that provide placement for RF cables. The cables are constructed with OSSP connectors on one end for direct contact to the DUT Interface Board (DIB), and SMA connectors on the other end for connect to the instrument(s). OSSP RF connectors are spring-loaded; SMA connectors are threaded.

Installation of DUT Interface Board

There are three guide posts on the Split Interface Plate to align the position of the DUT interface board for installation.

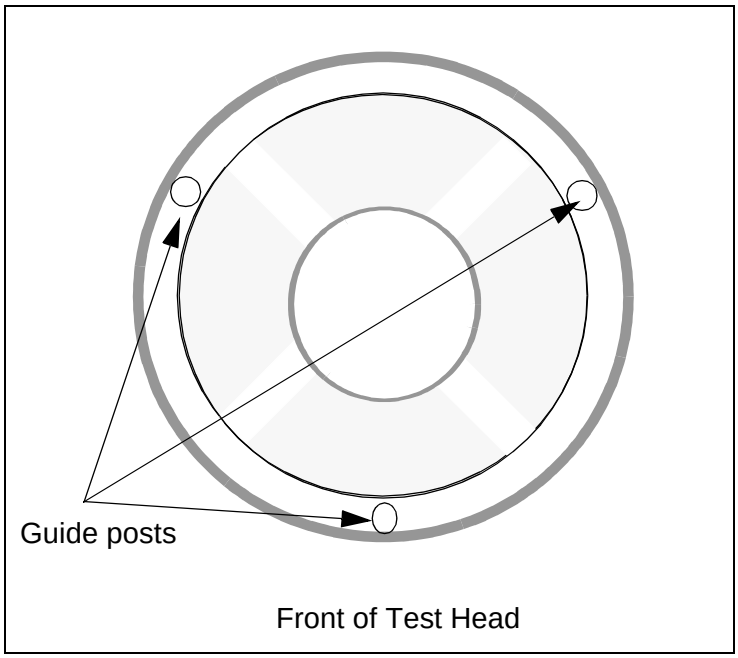

Figure 2.5: Guide Posts For Installing DUT Interface Board

Removal of Outer Plate

The outer plate of the Split Interface Plate is securely attached to the System Configuration Module (SCM, also known as family board). If the SCM is removed from the test head, the outer ring is also extracted from the test head.

For more information on maintenance, refer to the Scheduled Maintenance manual.

Electrical Specifications

The following table shows the electrical specifications of the Split Ring Interface Plate.

Table 2.1: Electrical Specifications, Split Ring Interface Plate

Pin Type	Qty	Maximum Current	Contact Resistance (mOhm Max / Dev)	Maximum Voltage	Impedance (Ohms)	Maximum Operating Frequency
Digital Signal	1024	0.5A (3A)	50 / 20	100V	50	2GHz
Digital Ground	1024	0.5A (3A)	50 / 20	0V	n.a.	n.a.
RF	16	n.a.	n.a.	800V	50	6GHz
High Performance DC / Video	512*	1.5A (3A)	50 / 20	100V	50	500MHz
General Purpose *	512*	1.5A (3A)	50 / 20	100V	n.a.	10MHz

* There are 512 spring pins, any number of which can be defined by the user as either High Performance DC / Video pins, or as default General Purpose pins.

Digital System Configuration Module (DSCM)

The Digital System Configuration Module (DSCM) provides user-definable connections from all Fusion instruments to the Split Ring Interface Plate. The Fusion instruments include CPS, PPS, Control Bit (CBIT), Sequenced Measure System (SMS), Wide Band sampler (WBS), Central Time Measurement Unit (CTMU), Digital Voltmeter (DVM), Arbitrary Waveform Source (AWS), RF boards, and user boards (breadboards for user-defined circuits).

For DC parametric measurements, the DSCM can be configured for 512 connections to the device under test (DUT). Precision resistors are included for calibration and verification.

On the DSCM, a programmable logic device (CPLD) has spare registers and pins that can be used to control user circuitry in the breadboard areas. If necessary, the DSCM can be replaced with a user-defined and assembled SCM to interface with a specific DUT.

HINT The height of components added to the DSCM should not exceed the height of the board stiffener: 0.5" / 1.1cm. Exceeding this height limit reduces the available clearance for docking the test head to external instruments.

Figure 2.6, DSCM Layout, Top View provides a sketch of the top view of the DSCM. The drawing is not dimensionally accurate.

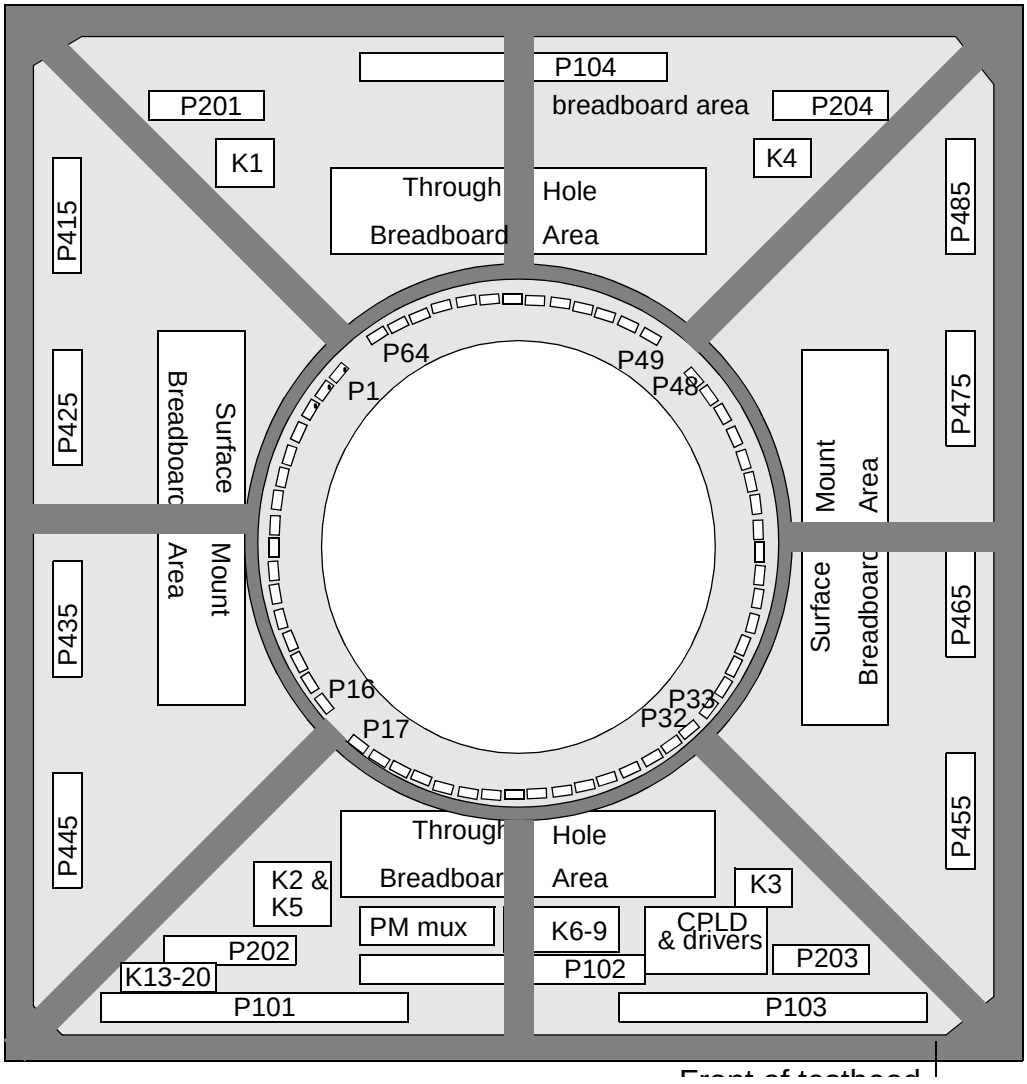

Figure 2.6: DSCM Layout, Top View

Table 2.2 describes the connectors illustrated in Figure 2.6, DSCM Layout, Top View, on page 2-7

Table 2.2: DSCM Components

Components	Description
P101 - P104	Connectors
P201 - P204	Connectors
K1 - K28	Relays
P1 - P64	Connectors: Default DSCM signals, or user-defined signals, to the outer plate of Split Interface Board

Table 2.2: DSCM Components (Continued)

Components	Description
P415, P425, P435, P445, P455, P465, P478, P485	Locations for optional modules: RF, CPS, PPS

Default DSCM Signal Connections

The connectors on the DSCM, which can be connected to the general purpose (GP) pins of the Split Ring Interface Plate, provide signal paths.

Following is a summary of the default DSCM connections. For the detailed list of DSCM input/output (I/O) signals, refer *Table 2.10, DSCM Default Connections to Outer Plate of Split Interface Plate, on page 2-18*.

Table 2.3: Instrument Connections, DSCM to Split Interface Plate Outer Ring

Functionality	Locked **	Instance	Connection Type	Pins ***
Analog pin	NO	1-16	1 GP: Force 1 GP: Sense or for Guard (ground)	32 GP
CBIT (from SCM: System Configuration Module)	NO	1-32	1 GP	32 GP
DPS / CPS / PPS* DSP: Device Power Source CPS: Controlled Power Supply PPS: Pulsed Power Supply	NO	1-24	3 pins: Force High 1 pin: Sense High 2 pins: Force Low 1 pin: Parallel Control	168 GP
SMS (Sequenced Measure System)	NO	1-8	2 pins: Measure 2 pins: Force 4 pins: Guard	32 SP
TH_Matrix (DVM)	NO	1	2 pins: Sense 2 pins: Guard	2 SP
DZ (THRG) (DZ: Digital Zero)	YES	1	1 pin: DZ 1 pin: Guard	2 GP
Serial Bus	YES	1	5 GP	5GP
EEPROM Bus (EEPROM: Electrically Erasable Programmable Only Memory)	YES	1	4 GP	4 GP

Table 2.3: Instrument Connections, DSCM to Split Interface Plate Outer Ring (Continued)

Functionality	Locked **	Instance	Connection Type	Pins ***
USRPWR	YES	+5	2 GP	15 GP
		-5.2	2 GP	
		+12	1 GP	
		+ / - 15	2 GP	
		+ / - 40	2 GP	
		RET	6 GP	
AWS1000 (slot 32)	NO	1	2 RF	2 RF
(AWS: Analog Waveform Source)			4 pins + 4 shields	4 GP
			4 SP	4 SP
WBS (Wide Band Sample) (slot 33 and slot 34)	NO	1 - 2	2 RF	4 RF
			17 GP	34 GP
CTMU+ / ACPMU	NO	1	2 RF	2 RF
			2 pins + 2 shields	2 SP
RF User Card (slot 3)	NO	1	2 RF	2 RF
			14 GP	24 GP
			4 pins + 4 shields	4 SP
HF User Card (SMS slots 30, 31)	NO	1 - 2	12 GP	24 GP
			4 pins + 4 shields	8 SP
DPAUX	NO	1 - 32	1 pin + 1 shield	32 SP

* The DPS lines tracing back to the mainframe are tied directly to the corresponding CPS / PPS lines on the DSCM: You cannot use both DPSs and CPSs in the same system if you are using the DSCM.

****** The devices that are marked locked in Table 2.3 should be connected as indicated: Changing the wiring to those devices can cause problems.

*** The GP and SP pins are located on the Split Interface Plate.

DC Measurement

The DSCM allows for DC measurements of the DUT.

Serial Bus. The DC measurement multiplexer (mux) is controlled by the serial bus. There is a programmable logic device (CPLD) on the DSCM that decodes the serial bus and drives the DC measurement multiplex relays. The CPLD has spare registers and pins that can be set to control user-defined circuitry in the breadboard area.

Analog Resources. The DSCM provides the standard DC measurement mux that connects the Digital Pins to the analog central resources for DC measurements, and for calibration. A set of precision resistors are provided for calibration and verification.

DSCM Relay Connections

The default connections of the DSCM can mate directly to the general purpose pins of the Split Ring Interface Plate. Programmable relays for DUT interface can perform the following:

- Switch between digital channels and analog channels
- Connect the Analog Pin Matrix bits to the Test Head Matrix bus and to the Digital Pin Matrix bus
- Connect the Pulsed Power Supply (PPS, optional module) to the Test Head Matrix bus
- Connect the Digital Voltmeter (DVM) to the Test Head Matrix bus
- Control the SMS relays

DSCM Relays

Relays enable connections from the PECHF measurement busses to several tester instruments. The possible relay connections are shown in Figure 2.7, Connection of PECHF Test Pins to Instruments, on page 2-12.

The Digital Pin cards (DP) each have two lines, through DPAUX, going up to the DSCM (or user-defined SCM): DP_MTX0, and DP_MTX1. The connections are user-defined:

- DP_MTX0 can be tied directly to any even numbered pin on the Pin Electronics Card (PECHF).
- DP_MTX1 can be tied directly to any odd-numbered pin on the PECHF.

The DP_MTX0 lines are tied together in quadrants (groups of 16 boards) on the DSCM, as are the DP_MTX1 lines. These quadrant connections can then be tied into the test head matrix (TH_MTX) via relays on the DSCM. The TH_MTX is an analog bus that resides on the DSCM.

The TH_MTX also has a relay connection to the AP_MTX for all 64 Analog Pins. The AP_MTX allows a force and a sense connection from any analog pin. For a full description of the AP_MTX, refer to the online manual.

The CPS / PPS lines are connected to the corresponding DPS lines on the DSCM. Either the CPS / PPS or DPS instrument can be used.

NOTE CPS / PPS and DPS can not be used simultaneously.

For central parametric measurement unit (PMU) capability, either Constant Power Supply (CPS), Pulsed Power Supply (PPS), or Device Power Source (DPS) can also be connected to the TH_MTX.

To calibrate the per-pin PMUs on the digital pin cards (DP PPMUs) there are two precision resistors: 1M-ohm and 10M-ohm. For more information on maintenance, refer to the online manual.

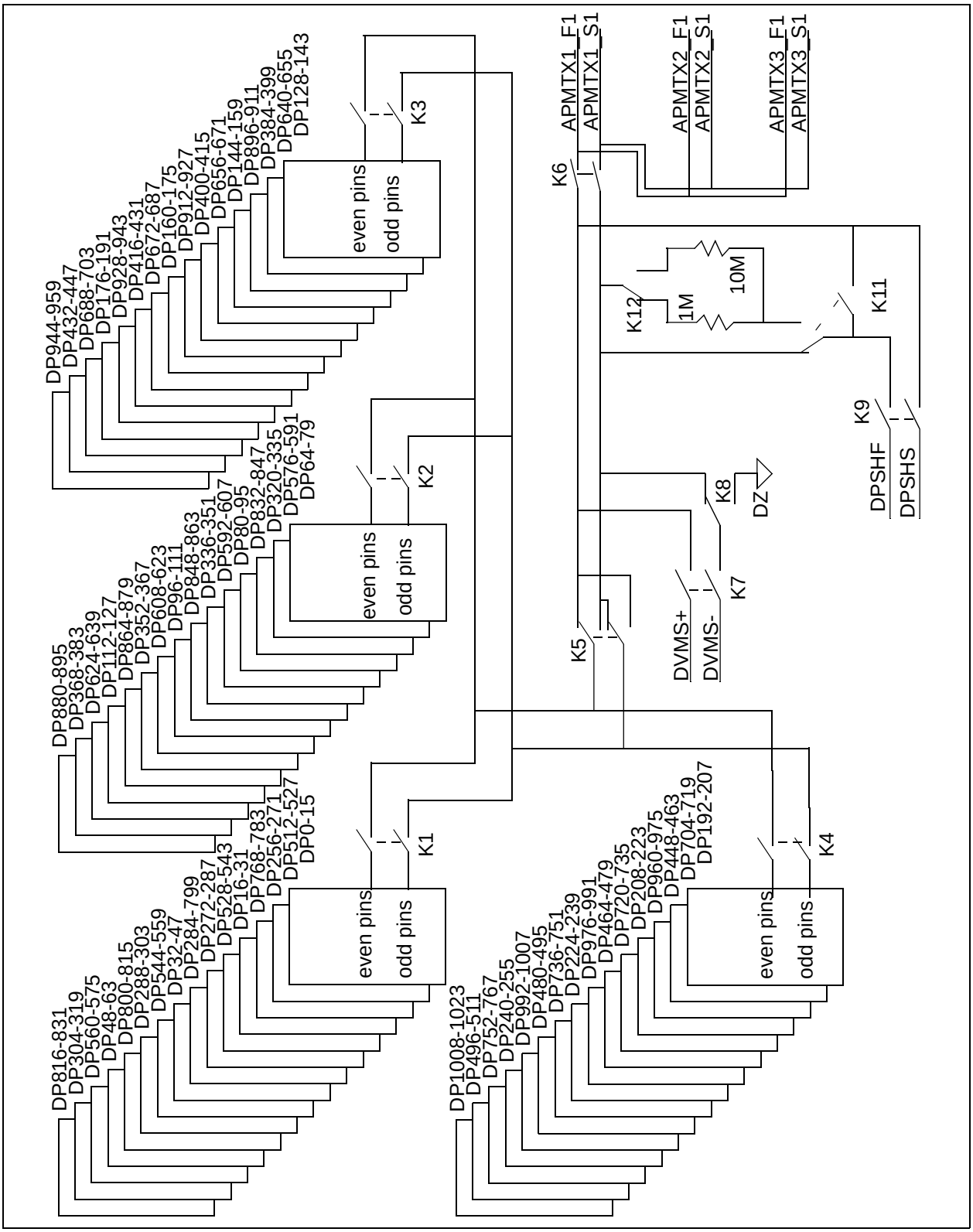

Figure 2.7: Connection of PECHF Test Pins to Instruments

SCM 1. Relays K1 through K5 switch between the digital channels and the analog channels. To set these relays, the Write Protect of Bit 5 must be set high.

Relay K6, when closed, connects the Analog Pin Matrix to the Test Head Matrix and to the Digital Pin Matrix busses.

Table 2.4: System Configuration Module 1

Bit	7	6	5	4	3	2	1	0
Relay / Write Protect	WP	K6	WP	K5	K4	K3	K2	K1

SCM 2. Relays K7 and K8 connect the DVM to the Test Head Matrix Bus. To set these relays, the Write Protect of Bit 2 must be set high.

Relays K9 through K12 connect the PPS to the Test Head Matrix bus. To set these relays, the Write Protect of Bit 7 must be set high.

Table 2.5: System Configuration Module 2

Bit	7	6	5	4	3	2	1	0
Relay / Write Protect	WP	K12	K11	K10	K9	WP	K8	K7

SCM 3 and SCM 4. Relays K13 - K20 (SCM 3) and K21 - K28 (SCM 4) control the SMS relays.

- K13, K17, K21, and K25 can be used to switch SMS1 and SMS2 for either direct connection to the DUT, or to multiplex through three SMSs.
  - SMS1 connects to SMS3, SMS5, and SMS 7.
  - SMS2 connects to SMS4, SMS6, and SMS8.

Table 2.6: System Configuration Module 3

Bit	7	6	5	4	3	2	1	0
Relay	K20	K19	K18	K17	K16	K15	K14	K13

Following is the table for SCM 4.

Table 2.7: System Configuration Module 4

Bit	7	6	5	4	3	2	1	0
Relay	K20	K19	K18	K17	K16	K15	K14	K13

SCM 5 . Relays K21 - K28, the PMCBITS, control the ECL multiplexer for the PaceMaker from the DUT. When PCMBIT1 and PMCBIT2 are set low, PM1 from the DUT goes out to the PaceMaker.

Table 2.8: System Configuration Module 5

Bit	7	6	5	4	3	2	1	0
Relay	K28	K27	K26	K25	K24	K23	K22	K21

THMUX Bus Connections

The following describes some common functions that can be performed by setting up THMUX bus connections through the DSCM.

To view the locations of the relays, refer to Figure 2.6, DSCM Layout, Top View, on page 2-7.

- Calibrate per pin parametric measurement unit (PPMU) Voltage Measurement:

  Force a voltage with the CPS (or DPS) and measure it with the PPMU (no current). Close relays K9 and K10. Close K1 through K5 as required to connect to pin.

- Calibrate PPMU Voltage Force:

  Force a voltage with the PPMU, and measure with the PPMU. No DSCM connections required.

- Calibrate PPMU Current Measurement For Higher PPMU Current Ranges:

  Force a current with the CPS (DPS) and a voltage with the PPMU. Measure the current with the PPMU. Close relay K9 and K10 and K1 through K5 as required to connect to pin. Make the kelvin connection on the pin card.

- Calibrate PPMU Current Measurement For Lower PPMU Current Ranges:

Force a voltage with the CPS (or DPS) through the calibration resistors on the DSCM load board. Force a voltage with the PPMU and measure the current with the PPMU. Close relays K9, K10, and K11; close K1 through K5 as required to connect to the test pin, and K12 to select which calibration resistor (1M-ohm or 10M-ohm.

The following is only a list of possible functions: Descriptions of how the connections are made are not included.

- Measure voltage on pin with DVM.
- Measure differential voltage on two pins with DVM.
- Measure voltage or current with the CPS (or DPS).
- Measure voltage and / or current with Analog pin.

HF/RF User Board Connections

The DSCM has connections directly to the Split Interface Plate from boards in the test head analog crate: SMS Cards 3, 30, 31. HF User Cards 30 - 31 have a total of 20 connections to the Split Interface Plate. The AUX signal of the DP is a relatively high-bandwidth (>100MHz) path that connects a signal from the SCM through a relay to the digital pin (DP) on a pin electronics card.

RF User Board 3 has 25 connections to the spring pins.

Table 2.9 shows the available number of connections to RF user cards: These connections are optional.

Table 2.9: RF User Card Connections

Instrument	Instance	Connection Type	Total Pins
RF User Board	1-3	2 RF	6 RF
		4 GP	12 GP
		8 pins + 8 shields	24 SP
RF User Board	4	2 RF	2 RF
		12 GP	12 GP
		4 pins + 4 shields	4 SP

For information on HF (high frequency)/RF (radio frequency) User Cards, refer to the online manual.

SMS Connections

The 8 SMS instruments in the test head analog crate have spring pins assigned to them on the DUT interface plate. For each of these first two SMSs, there is a pair of relays to establish connection: 1 relay for +/- source; 1 relay for +/-measurement.

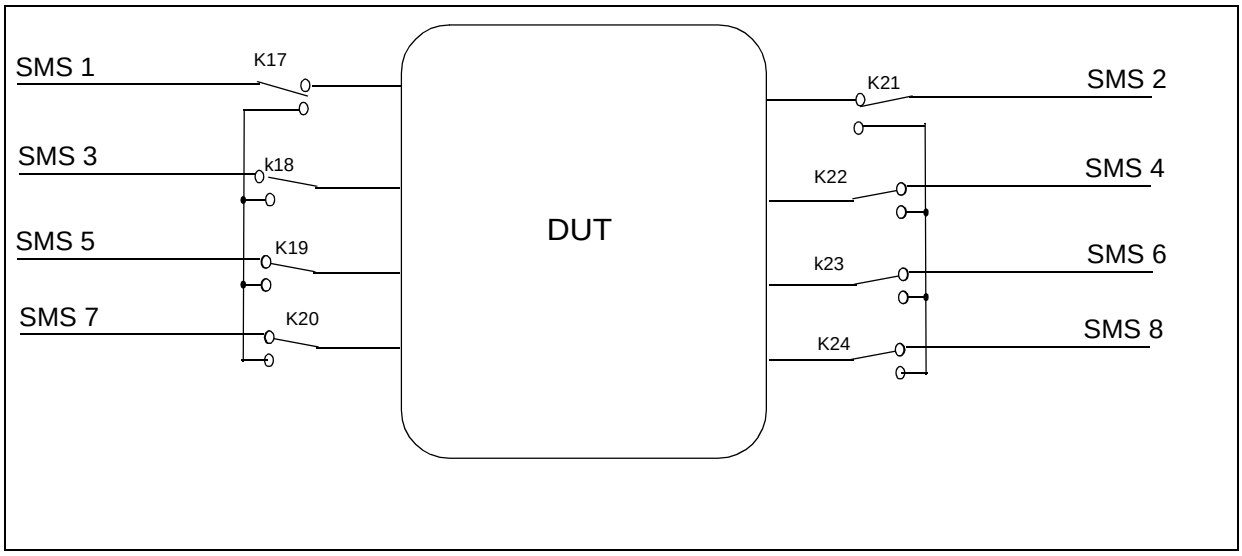

Figure 2.8: SMS 1:4 Multiplex Connections

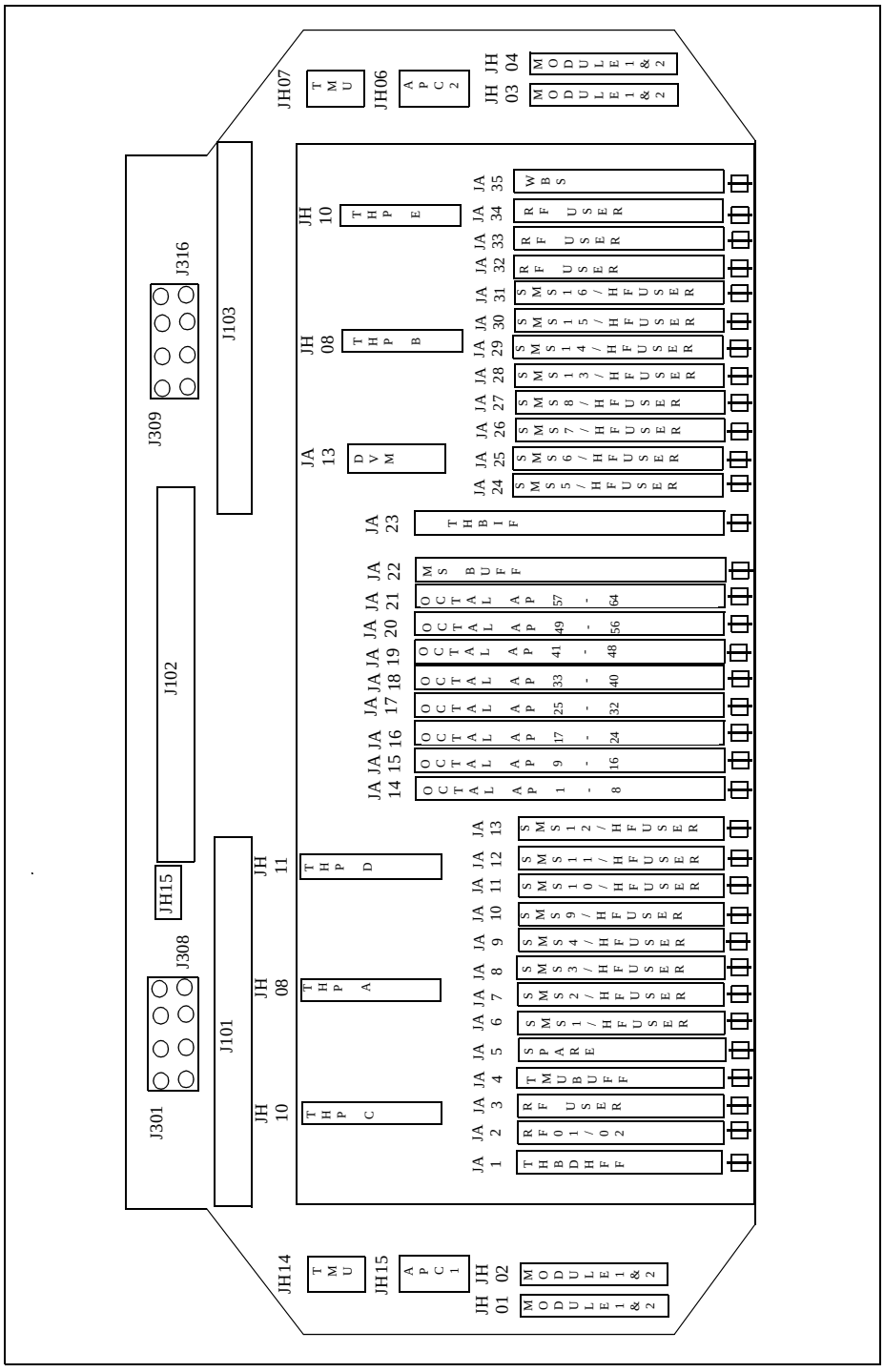

Figure 2.9: Fusion HF Test Head Analog Backplane

Instrument Connections to Split Interface Plate

The following instruments can be connected to the Split Interface Plate through the DSCM board. The Split Interface Plate has 512 General Purpose (GP) pins and 16 RF connectors.

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate

Connector	Signal Name : Description	Connector	Signal Name : Description
P1 – 1	SH1 :Sense High, DPS1	P1 – 2	SH17 : Sense High, DPS17
P1 – 3	FH1 : Force High, DPS1	P1 – 4	FH17 : Force High, DPS17
P1 – 5	FH1 : Force High, DPS1	P1 – 6	FH17 : Force High, DPS17
P1 – 7	FH1 : Force High, DPS1	P1 – 8	FH17 : Force High, DPS17
P2 – 1	FL1–2 : Force Low, DPS1 & DPS2	P2 – 2	FL17–18 : Force Low, DPS17 & DPS18
P2 – 3	FL1–2 : Force Low, DPS1 & DPS2	P2 – 4	FL17–18 : Force Low, DPS17 & DPS18
P2 – 5	FL1–2 : Force Low, DPS1 & DPS2	P2 – 6	FL17–18 : Force Low, DPS17 & DPS18
P2 – 7	FL1–2 : Force Low, DPS1 & DPS2	P2 – 8	FL17–18 : Force Low, DPS17 & DPS18
P3 – 1	FH2 : Force High, DPS2	P3 – 2	FH18 : Force High, DPS18
P3 – 3	FH2 : Force High, DPS2	P3 – 4	FH18 : Force High, DPS18
P3 – 5	FH2 : Force High, DPS2	P3 – 6	FH18 : Force High, DPS18
P3 – 7	SH2 : Sense High, DPS2	P3 – 8	SH18 : Sense High, DPS18
P4 – 1	+5V : Utility Supply +5V	P4 – 2	U30_IC_9 : User 30 Interconnect 9
P4 – 3	CBIT1 : CBIT 1	P4 – 4	CBIT2 : Control Bit 2
P4 – 5	CBIT3 : CBIT 3	P4 – 6	CBIT4 : Control Bit 4
P4 – 7	AP_G_S[1] : ana1og pin guard sense [1]	P4 – 8	AP[1] : ana1og pin [1]
P5 – 1	+15V : Utility Supply +15V	P5 – 2	U30_IC_10 : User 30 Interconnect 10
P5 – 3	CBIT17 : C Control Bit 17	P5 – 4	CBIT18 : Control Bit 18
P5 – 5	CBIT19 : Control Bit 19	P5 – 6	CBIT20 : Control Bit 20
P5 – 7	AP_G_S[2] : ana1og pin guard sense [2]	P5 – 8	AP[2] : ana1og pin [2]
P6 – 1*	GND : Ground	P6 – 2*	SMS1M+ : SMS1 Measure +

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P6 – 3*	SMS1M– : SMS1 Measure –	P6 – 4*	GND : Ground
P6 – 5*	GND : Ground	P6 – 6*	SMS1S+ : SMS1 Source +
P6 – 7*	SMS1S– : SMS1 Source –	P6 – 8*	GND : Ground
P7 – 1*	GND : Ground	P7 – 2*	SMS2M+ : SMS2 Measure +
P7 – 3*	SMS2M– : SMS2 Measure –	P7 – 4*	GND : Ground
P7 – 5*	GND : Ground	P7 – 6*	SMS2S+ : SMS2 Source +
P7 – 7*	SMS2 Source –	P7 – 8*	GND : Ground
P8 – 1	GND : Ground	P8 – 2	EE_+5V : EEPROM +5V
P8 – 3	DZ : Digital Zero (guard / sense)	P8 – 4	GND : Ground
P8 – 5	EE_DATA : EEPROM data	P8 – 6	EE_CLK : EEPROM clock
P8 – 7	U3_IC_15 : User 3 Interconnect 15	P8 – 8	U3_IC_16 : User 3 Interconnect 16
P9 – 1*	GND : Ground	P9 – 2*	SMS9M+ : SMS9 Measure +
P9 – 3*	DPAUX256 : Digital pin auxiliary**	P9 – 4*	GND : Ground
P9 – 5*	GND : Ground	P9 – 6*	DPAUX16 : Digital pin auxiliary**
P9 – 7*	SMS9 Source –	P9 – 8*	GND : Ground
P10 – 1*	GND : Ground	P10 – 2*	DPAUX32 : Digital pin auxiliary**
P10 – 3*	DPAUX288 : Digital pin auxiliary**	P10 – 4*	GND : Ground
P10 – 5*	GND : Ground	P10 – 6*	DPAUX48 : Digital pin auxiliary**
P10 – 7*	DPAUX272 : Digital pin auxiliary**	P10 – 8*	GND : Ground
P11 – 1	–5V : Utility Supply –5V	P11 – 2	GND : Ground
P11 – 3	PS_PP1 : Power Supply 1 Parallel Control	P11 – 4	PS_PP17 : Power Supply 17 Parallel Control
P11 – 5	PS_PP2 : Power Supply 2 Parallel Control	P11 – 6	PS_PP18 : Power Supply 18 Parallel Control
P11 – 7	AP_G_S[9] : Ana1og pin guard sense [9]	P11 – 8	AP[9] : Aana1og pin [9]
P12 – 1	–15 : Utility Supply –15V	P12 – 2	GND : Ground

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P12 – 3	PS_PP9 : Power Supply 9 Parallel Control	P12 – 4	PS_PP19 : Power Supply 19 Parallel Control
P12 – 5	PS_PP10 : Power Supply 10 Parallel Control	P12 – 6	PS_PP20 : Power Supply 20 Parallel Control
P12 – 7	AP_G_S[10] : Ana1og pin guard sense [10]	P12 – 8	AP[10] : Ana1og pin [10]
P13 – 1*	THGRD+ : TH Guard	P13 – 2*	TH_MTX2 : TH Matrix
P13 – 3*	CTMU1	P13 – 4*	GND
P13 – 5*	THGRD+ : TH Guard	P13 – 6*	TH_MTX1 : TH Matrix
P13 – 7*	CTMU2	P13 – 8*	GND
P14 – 1	SH9 : Sense High, DPS9	P14 – 2	SH19 : Sense High, DPS19
P14 – 3	FH9 : Force High, DPS9	P14 – 4	FH19 : Force High, DPS19
P14 – 5	FH9 : Force High, DPS9	P14 – 6	FH19 : Force High, DPS19
P14 – 7	FH9 : Force High, DPS9	P14 – 8	FH19 : Force High, DPS19
P15 – 1	FL9–10 : Force Low, DPS9 & DPS10	P15 – 2	FL19–20 : Force Low, DPS19 & DPS20
P15 – 3	FL9–10 : Force Low, DPS9 & DPS10	P15 – 4	FL19–20 : Force Low, DPS19 & DPS20
P15 – 5	FL9–10 : Force Low, DPS9 & DPS10	P15 – 6	FL19–20 : Force Low, DPS19 & DPS20
P15 – 7	FL9–10 : Force Low, DPS9 & DPS10	P15 – 8	FL19–20 : Force Low, DPS19 & DPS20
P16 – 1	FH10 : Force High, DPS10	P16 – 2	FH20 : Force High, DPS20
P16 – 3	FH10 : Force High, DPS10	P16 – 4	FH20 : Force High, DPS20
P16 – 5	FH10 : Force High, DPS10	P16 – 6	FH20 : Force High, DPS20
P16 – 7	SH10 : Sense High, DPS10	P16 – 8	SH20 : Sense High, DPS20
P17 – 1	SH3 : Sense High, DPS3	P17 – 2	SH11 : Sense High, DPS11
P17 – 3	FH3 : Force High, DPS3	P17 – 4	FH11 : Force High, DPS11
P17 – 5	FH3 : Force High, DPS3	P17 – 6	FH11 : Force High, DPS11
P17 – 7	FH3 : Force High, DPS3	P17 – 8	FH11 : Force High, DPS11
P18 – 1	Force Low, DPS3 & DPS4	P18 – 2	FL11–12 : Force Low, DPS11 & DPS12

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P18 – 3	FL3–4 : Force Low, DPS3 & DPS4	P18 – 4	FL11–12 : Force Low, DPS11 & DPS12
P18 – 5	FL3–4 : Force Low, DPS3 & DPS4	P18 – 6	FL11–12 : Force Low, DPS11 & DPS12
P18 – 7	FL3–4 : Force Low, DPS3 & DPS4	P18 – 8	FL11–12 : Force Low, DPS11 & DPS12
P19 – 1	FH4 : Force High, DPS4	P19 – 2	FH12 : Force High, DPS12
P19 – 3	FH4 : Force High, DPS4	P19 – 4	FH12 : Force High, DPS12
P19 – 5	FH4 : Force High, DPS4	P19 – 6	FH12 : Force High, DPS12
P19 – 7	SH4 : Sense High, DPS4	P19 – 8	SH12 : Sense High, DPS12
P20 – 1	U3_IC_17 : User 3 Interconnect 17	P20 – 2	U3_IC_18 : User 3 Interconnect 18
P20 – 3	CBIT5 : Control Bit 5 (CBIT A02)	P20 – 4	CBIT6 : Control Bit 6 (CBIT B02)
P20 – 5	CBIT7 : Control Bit 7 (CBIT A03)	P20 – 6	CBIT8 : CBIT 8 (CBIT B03)
P20 – 7	AP_G_S[3]: Ana1og pin guard / sense [3]	P20 – 8	AP[3] : Ana1og pin 3
P21 – 1	U3_IC_19 : User 3 Interconnect 19	P21 – 2	U3_IC_20 : User 3 Interconnect 20
P21 – 3	CBIT21 : CBIT 21 (CBIT A18)	P21 – 4	CBIT22 : Control Bit 22 (CBIT B18)
P21 – 5	CBIT23 : CBIT 23 (CBIT A19)	P21 – 6	CBIT24 : Control Bit 24 (CBIT B19)
P21 – 7	AP_G_S[4]: ana1og pin guard / sense [4]	P21 – 8	AP[4]: ana1og pin [4]
P22 – 1*	GND : Ground	P22 – 2*	SMS3M+ : SMS3 Measure +
P22 – 3*	SMS3M– : SMS3 Measure –	P22 – 4*	GND : Ground
P22 – 5*	GND : Ground	P22 – 6*	SMS3S+ : SMS3 Source +
P22 – 7*	SMS3S– : SMS3 Source –	P22 – 8*	GND : Ground
P23 –1 *	GND : Ground	P23 –2*	SMS4M+ : SMS4 Measure +
P23 – 3*	SMS4M– : SMS4 Measure –	P23 – 4*	GND : Ground
P23 – 5*	GND : Ground	P23 – 6*	SMS4S+ : SMS4 Source +
P23 – 7*	SMS4S– : SMS4 Source –	P23 – 8*	GND : Ground
P24 – 1*	GND : Ground	P24 – 2*	PM1 – DUT : Pacemaker1 – DUT

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P24 – 3*	PM1 – DUT* : Pacemaker – DUT*	P24 – 4*	GND : Ground
P24 – 5*	GND : Ground	P24 – 6*	DUT – PM : DUT – Pacemaker
P24 – 7*	DUT – PM* : DUT – Pacemaker*	P24 – 8*	GND : Ground
P25 – 1*	GND : Ground	P25 – 2*	DPAUX64 : Digital pin auxiliary**
P25 – 3*	DPAUX320 : Digital pin auxiliary**	P25 – 4*	GND : Ground
P25 – 5*	GND : Ground	P25 – 6*	DPAUX80 : Digital pin auxiliary**
P25 – 7*	DPAUX336 : Digital pin auxiliary**	P25 – 8	GND : Ground
P26 – 1*	GND : Ground	P26 – 2*	DPAUX96 : Digital pin auxiliary**
P26 – 3*	DPAUX352 : Digital pin auxiliary*8	P26 – 4*	GND : Ground
P26 – 5*	GND : Ground	P26 – 6*	DPAUX122 : Digital pin auxiliary**
P26 – 7*	DPAUX368 : Digital pin auxiliary**	P26 – 8*	GND : Ground
P27 – 1	U31_IC_9 : User 31 Interconnect 9	P27 – 2	GND : Ground
P27 – 3	PS_PP3 : Power Supply 3 Parallel Control	P27 – 4*	PS_PP19 : Power Supply 19 Parallel Control
P27 – 5	PS_PP4 : Power Supply 4 Parallel Control	P27 – 6	PS_PP20 : Power Supply 20 Parallel Control
P27 – 7	AP_G_S[11] : ana1og pin guard / sense [11]	P27 – 8	AP[11] : ana1og pin [11]
P28 – 1	WBS2arm : Wide Band Sampler trigger	P28 – 2	+12V : Utility Supply +12V
P28 – 3	UO3_IC_21 : User 03 Interconnect 21	P28 – 4	UO3_IC_22 : User 03 Interconnect 22
P28 – 5	UO3_IC_23 : User 03 Interconnect 23	P28 – 6	UO3_IC_24 : User 03 Interconnect 24
P28 – 7	AP_G_S[12] : ana1og pin guard / sense [12]	P28 – 8	AP[12] : ana1og pin [12]
P29 – 1*	GND : Ground	P29 – 2*	SMS15M+ : SMS measure

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P29 – 3*	SMS15M– : SMS measure	P29 – 4*	GND : Ground
P29 – 5*	GND : Ground	P29 – 6*	SMS15S+ : SMS source
P29 – 7*	SMS15S– : SMS source	P29 – 8*	GND : Ground
P30 – 1*	U3_IC_5 : User 3 Interconnect 5	P30 – 2*	U3_IC_6 : User 3 Interconnect 6
P30 – 3*	U3_IC_7 : User 3 Interconnect 7	P30 – 4*	U3_IC_8 : User 3 Interconnect 8
P30 – 5*	U3_IC_9 : User 3 Interconnect 9	P30 – 6*	U3_IC_10 : User 3 Interconnect 5 : User 3 Interconnect 10
P30 – 7*	U3_IC_11 : User 3 Interconnect 11	P30 – 8*	U3_IC_12 : User 3 Interconnect 12
P31 – 1	WBS2swp* : WBS swap*	P31 – 2	WBS2swp : WBS swap
P31 – 3	WBS2extclk* : WBS external clock *	P31 – 4	WBS2extclk : WBS external clock
P31 – 5	WBS2cmpclk* : WBS comparator clock*	P31 – 6	WBS2cmplk : WBS comparator clock
P31 – 7	WBS2intclk* : WBS internal clock *	P31 – 8	WBS2intlck : WBS2 internal clock
P32 – 1	WBS2cmp1* : WBS cmp1	P32 – 2	WBS22cmp1 : WBS2 cmpl
P32 – 3	WBS2ana1 : WBS2 ana1og	P32 – 4	WBS2cmp1_fb : WBS2 cmpl_fb
P32 – 5	WBS2cmp2*: WBS2 cmp2	P32 – 6	WBS2cmp2 : WBS2 cmp2
P32 – 7	WBS2ana2: WBS2 ana1og	P32 – 8	WBS2cmp2_fb : WBS2 cmp2_fb
P33 –1	SH5 : Sense High, DPS5	P33 –2	SH21 : Sense High, DPS21
P33 – 3	FH5 : Force High, DPS5	P33 – 4	FH21 : Force High, DPS21
P33 – 5	FH5 : Force High, DPS5	P33 – 6	FH21 : Force High, DPS21
P33 – 7	FH5 : Force High, DPS5	P33 – 8	FH21 : Force High, DPS21
P34 – 1	FL5–6 : Force Low, DPS5 & DPS6	P34 – 2	FL21–22 : Force Low, DPS21 & DPS22
P34 – 3	FL5–6 : Force Low, DPS5 & DPS6	P34 – 4	FL21–22 : Force Low, DPS21 & DPS22
P34 – 5	FL5–6 : Force Low, DPS5 & DPS6	P34 – 6	FL21–22 : Force Low, DPS21 & DPS22
P34 – 7	FL5–6 : Force Low, DPS5 & DPS6	P34 – 8	FL21–22 : Force Low, DPS21 & DPS22
P35 – 1	FH6 : Force High, DPS6	P35 – 2	FH22 : Force High, DPS22

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P35 – 3	FH6 : Force High, DPS6	P35 – 4	FH22 : Force High, DPS22
P35 – 5	FH6 : Force High, DPS6	P35 – 6	FH22 : Force High, DPS22
P35 – 7	SH6 : Sense High, DPS6	P35 – 8	SH22 : Sense High, DPS22
P36 –1	+5V Utility Supply +5V	P36 –2	U03_IC_17 : User 03 Interconnect 17
P36 – 3	CBIT9 : Control Bit 9 (CBIT A04)	P36 – 4	CBIT10 : Control Bit 10 (CBIT B04)
P36 – 5	CBIT11 : Control Bit 11 (CBIT A05)	P36 – 6	CBIT12 : Control Bit 12 (CBIT B05)
P36 – 7	AP_G_S[5] : ana1og pin guard / sense [5]	P36 – 8	AP[5] : ana1og pin [5]
P37 – 1	+40V : Utility Supply +40V	P37 – 2	U03_IC_18 : User 3 Interconnect 18
P37 – 3	CBIT25 : Control Bit 25	P37 – 4	CBIT26 : Control Bit 26
P37 – 5	CBIT27 : Control Bit 27	P37 – 6	CBIT28 : Control Bit 28
P37 – 7	AP_G_S[6] : ana1og pin guard / sense [6]	P37 – 8	AP[6] : ana1og pin [6]
P38 – 1*	GND : Ground	P38 – 2*	SMS5M+ : SMS5 Measure +
P38 – 3*	SMS5M– : SMS5 Measure –	P38 – 4*	GND : Ground
P38 – 5*	GND : Ground	P38 – 6*	SMS5S+ : SMS5 Source +
P38 – 7*	SMS5S– : SMS5 Source –	P38 – 8*	GND : Ground
P39 – 1*	GND : Ground	P39 – 2*	SMS6M+ : SMS6 Measure +
P39 – 3*	SMS6M– : SMS6 Measure –	P39 – 4*	GND : Ground
P39 – 5*	GND : Ground	P39 – 6*	SMS6S+ : SMS6 Source +
P39 – 7*	SMS6S– : SMS6 Source –	P39 – 8*	GND : Ground
P40 – 1	U3_IC_1 : User 3 Interconnect 1	P40 – 2	U3_IC_2 : User 3 Interconnect 2
P40 – 3	U3_IC_3 : User 3 Interconnect 3	P40 – 4	U3_IC_4 : User 3 Interconnect 4
P40 – 5	U30_IC_1 : User 30 Interconnect 1	P40 – 6	U30_IC_2 : User 30 Interconnect 2
P40 – 7	U30_IC_3 : User 30 Interconnect 3	P40 – 8	U30_ICS_4 : User 30 Interconnect 4
P41 – 1*	GND : Ground	P41 – 2*	DPAUX128 : Digital pin auxiliary**

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P41 – 3*	DPAUX382 : Digital pin auxiliary**	P41 – 4*	GND : Ground
P41 – 5*	GND : Ground	P41 – 6*	DPAUX144 : Digital pin auxiliary**
P41 – 7*	DPAUX400 : Digital auxiliary**	P41 – 8*	GND : Ground
P42 – 1*	GND : Ground	P42 – 2*	DPAUX160 : Digital auxiliary**
P42 – 3*	DPAUX416 : Digital auxiliary	P42 – 4*	GND : Ground
P42 – 5*	GND : Ground	P42 – 6*	DPAUX176 : Digital auxiliary
P42 – 7*	DPAUX432 : Digital auxiliary	P42 – 8*	GND : Ground
P43 –1	–5V : Utility Supply –5V	P43 –2	GND : Ground
P43 – 3	PS_PP5 : Power Supply 5 Parallel Control	P43 – 4	PS_PP21 : Power Supply 21 Parallel Control
P43 – 5	PS_PP6 : Power Supply 6 Parallel Control	P43 – 6	PS_PP22 : Power Supply 22 Parallel Control
P43 – 7	AP_G_S[13] : ana1og pin guard / sense [13]	P43 – 8	AP[13] : ana1og pin [13]
P44 – 1	–40V : Utility Supply –40V	P44 – 2	GND : Ground
P44 – 3	PS_PP13 : Power Supply 13 Parallel Control	P44 – 4	PS_PP29 : Power Supply 29 Parallel Control
P44 – 5	PS_PP14 : Power Supply 14 Parallel Control	P44 – 6	PS_PP30 : Power Supply 30 Parallel Control
P44 – 7	AP_G_S[14] : ana1og pin guard / sense [14]	P44 – 8	AP[14] : ana1og pin [14]
P45 – 1	U30_IC_5 : User 30 Interconnect 5	P45 – 2	U30_IC_6 : User 30 Interconnect 6
P45 – 3	U30_IC_7 : User 30 Interconnect 7	P45 – 4	U30_IC_8 ; User 30 Interconnect 8
P45 – 5	AWS_br0 : AWS branch 0	P45 – 6	AWS_br1 : AWS branch 1
P45 – 7	AWS_br2 : AWS branch 2	P45 – 8	AWS_br3 : AWS branch 3
P46 – 1	SH13 : Sense High, DPS13	P46 – 2	SH23 : Sense High, DPS23
P46 – 3	FH13 : Force High, DPS13	P46 – 4	FH23 : Force High, DPS23
P46 – 5	FH13 : Force High, DPS13	P46 – 6	FH23 : Force High, DPS23
P46 – 7	FH13 : Force High, DPS13	P46 – 8	FH23 : Force High, DPS23

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P47 – 1	FL13–14 : Force Low, DPS13 & DPS14	P47 – 2	FL23–24 : Force Low, DPS23 & DPS24
P47 – 3	FL13–14 : Force Low, DP13 & DPS14	P47 – 4	FL23–24 : Force Low, DPS23 & DPS24
P47 – 5	FL13–14 : Force Low, DPS13 & DPS14	P47 – 6	FL23–24 : Force Low, DPS23 & DPS24
P47 – 7	FL13–14 : Force Low, DPS13 & DPS14	P47 – 8	FL23–24 : Force Low, DPS23 & DPS24
P48 – 1	FH14 : Force High, DPS14	P48 – 2	FH24 : Force High, DPS24
P48 – 3	FH14 : Force High, DPS14	P48 – 4	FH24 : Force High, DPS24
P48 – 5	FH14 : Force High, DPS14	P48 – 6	FH24 : Force High, DPS24
P48 – 7	SH14 : Sense High, DPS14	P48 – 8	SH24 : Sense High, DPS24
P49 – 1	SH7 : Sense High, DPS7	P49 – 2	SH15 : Sense High, DPS15
P49 – 3	FH7 : Force High, DPS7	P49 – 4	FH15 : Force High, DPS15
P49 – 5	FH7 : Force High, DPS7	P49 – 6	FH15 : Force High, DPS15
P49 – 7	FH7 : Force High, DPS7	P49 – 8	FH15 : Force High, DPS15
P50 – 1	FL7–8 : Force Low, DPS7 & DPS8	P50 – 2	FL15–16 : Force Low, DPS15 & DPS16
P50 – 3	FL7–8 : Force Low, DPS7 & DPS8	P50 – 4	FL15–16 : Force Low, DPS15 & DPS16
P50 – 5	FL7–8 : Force Low, DPS7 & DPS8	P50 – 6	FL15–16 : Force Low, DPS15 & DPS16
P50 – 7	FL7–8 : Force Low, DPS7 & DPS8	P50 – 8	FL15–16 : Force Low, DPS15 & DPS16
P51 – 1	FH8 : Force High, DPS8	P51 – 2	FH16 : Force High, DPS16
P51 – 3	FH8 : Force High, DPS8	P51 – 4	FH16 : Force High, DPS16
P51 – 5	FH8 : Force High, DPS8	P51 – 6	FH16 : Force High, DPS16
P51 – 7	SH8 : Sense High, DPS8	P51 – 8	SH16 : Sense High, DPS16
P52 – 1	U03_IC_13 : User 03 Interconnect 13	P52 – 2	U03_IC_14 : User 03 Interconnect 14
P52 – 3	CBIT13 : Control Bit 13	P52 – 4	CBIT14 : Control Bit 14
P52 – 5	CBIT15 : Control Bit 15	P52 – 6	CBIT16 : Control Bit 16
P52 – 7	AP_G_S[7] : Ana1og pin guard / sense [7]	P52 – 8	AP[7] : Ana1og pin [7]

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P53 – 1	U31_IC_1 : User 31 Interconnect 1	P53 – 2	U31_IC_2 : User 31 Interconnect 2
P53 – 3	CBIT29 : Control Bit 29	P53 – 4	CBIT30 : Control Bit 30
P53 – 5	CBIT31 : Control Bit 31	P53 – 6	CBIT32 : Control Bit 32
P53 – 7	AP_G_S[8] : ana1og pin guard / sense [8]	P53 – 8	AP[8] : ana1og pin [8]
P54 –1 *	GND : Ground	P54 – 2*	SMS7M+ : SMS7 Measure +
P54 – 3*	SMS7M– : SMS7 Measure –	P54 – 4*	GND : Ground
P54 – 5*	GND : Ground	P54 – 6*	SMS7S+ : SMS7 Source +
P54 – 7*	SMS7S– : SMS7 Source –	P54 – 8*	GND : Ground
P55 – 1*	GND : Ground	P55 – 2*	SMS8M+ : SMS8 Measure +
P55 – 3*	SMS8M– : SMS8 Measure –	P55 – 4*	GND : Ground
P55 – 5*	GND : Ground	P55 – 6*	SMS8S+
P55 – 7*	SMS8S– : SMS8 Source –	P55 – 8*	GND : Ground
P56 – 1	H_STB	P56 – 2	H_EN[5]
P56 – 3	H_CLK[0]	P56 – 4	H_RESET
P56 – 5	H_DATA	P56 – 6	U31_IC_9 : User 31 Interconnect 10
P56 – 7	U31_IC_11 : User 31Interconnect 11	P56 – 8	U31_IC_12 : User 31 Interconnect 12
P57 – 1*	GND : Ground	P57 – 2*	DPAUX192 : Digital pin auxiliary**
P57 – 3*	DPAUX448 : Digital pin auxiliary**	P57 – 4*	GND : Ground
P57 – 5*	GND : Ground	P57 – 6*	DPAUX208 : Digital pin auxiliary**
P57 – 7*	DPAUX464 : Digital pin auxiliary**	P57 – 8*	GND : Ground
P58 – 1*	GND : Ground	P58 – 2*	DPAUX224 : Digital pin auxiliary**
P58 – 3*	DPAUX480 : Digital pin auxiliary**	P58 – 4*	GND : Ground
P58 – 5*	GND : Ground	P58 – 6*	DPAUX240 : Digital pin auxiliary**

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P58 – 7 *	DPAUX496 : Digital pin auxiliary**	P58 – 8*	GND : Ground
P59 – 1	WBS1 arm : Wide Band Sample trigger	P59 – 2	GND : Ground
P59 – 3	PS_PP7 : Power Supply 7 Parallel Control	P59 – 4	PS_PP15 : Power Supply 15 Parallel Control
P59 – 5	PS_PP8 : Power Supply 8 Parallel Control	P59 – 6	PS_PP16 : Power Supply 16 Parallel Control
P59 – 7	AP_G_S[15] : ana1og pin guard / sense [15]	P59 – 8	AP[15] : ana1og pin [15]
P60 – 1	U31_IC_3 : User 31 Interconnect 3	P60 – 2	U31_IC_4 : User 31 Interconnect 4
P60 – 3	U31_IC_5 : User 31 Interconnect 5	P60 – 4	U31_IC_6 : User 31 Interconnect 6
P60 – 5	U31_IC_7 : User 31 Interconnect 7	P60 – 6	U31_IC_8 : User 31 Interconnect 8
P60 – 7	AP_G_S[16] : ana1og pin guard / sense [16]	P60 – 16	AP[16] : ana1og pin [16]
P61 – 1*	AWS_br_grd : AWS branch grd	P61 – 2*	AWS_br : AWS branch
P61 – 3*	AWS_adv : AWS advance	P61 – 4*	AWS_adv_grd : AWS advance grd
P61 – 5*	AWS_trig_grd : AWS trigger grd	P61 – 6*	AWS_trig : AWS trigger
P61 – 7*	AWS_mark : AWS mark	P61 – 8*	AWS_mark_grd : AWS mark grd
P62 – 1	GND : Ground	P62 – 2	SMS16M+
P62 – 3	SMS16M–	P62 – 4	GND : Ground
P62 – 5	GND : Ground	P62 – 6	SMS16S+
P62 – 7	SMS16M–	P62 – 8	GND : Ground
P63 – 1	WBS1swp* : Wide Band Sample swp*	P63 – 2	WBS1swp: Wide Band Sample swp
P63 – 3	WBS1extclk* : Wide Board Sample external clock*	P63 – 4	WBS1extclk : Wide Band Sample external clock
P63 – 5	WBS1cmp1cmpclk* : Wide Band Sample comparator clock*	P63 – 6	WBS1cmpclk : Wide Band Sample comparator clock
P63 – 7	WBS1intclk* : Wide Band Sample internal clock*	P63 – 8	WBS1intclk: Wide Band Sample internal clock

Table 2.10: DSCM Default Connections to Outer Plate of Split Interface Plate (Continued)

Connector	Signal Name : Description	Connector	Signal Name : Description
P64 – 1	WBS1cmpl* : Wide Band Sample comparator 1*	P63 – 2	WBS1 cpm1 : Wide Band Sample comparator 1
P64 – 3	WBS1ana1 : Wide Board Sample Analog 1	P63 – 4	WBS1compl_fb : Wide Band Sample comparator fb
P64 – 5	WBS1cmp2* : Wide Band Sample comparator 2*	P63 – 6	WBS1cmp2 : Wide Band Sample comparator
P64 – 7	WBS1ana2 : Wide Band Sample Analog	P63 – 8	WBS1cmp2_fb : Wide Band Sample compartor fb

* Coaxial connector (under the Connector column only).

** DPAUX# is for the PECHF board that is located in the slot with the pin number. Example: DPAUX256 is for the PECHF that is located in the slot which begins with pin 256.

User-Defined Control Bits

The following control bits (CBIT) are determined by the user. For detailed information about CBITs, refer to the online manual, *Linear Subsystem Hardware*.

Table 2.11 lists Control Bit 2.

Table 2.11: CONROL BIT 2

7	6	5	4	3	2	1	0
CBIT 16	CBIT 15	CBIT 14	CBIT 13	CBIT 12	CBIT 11	CBIT 10	CBIT 9

Table 2.12 lists Control Bit 3.

Table 2.12: CONTROL BIT 3

7	6	5	4	3	2	1	0
CBIT 24	CBIT 23	CBIT 22	CBIT 21	CBIT 20	CBIT 19	CBIT 18	CBIT 17

Table 2.13 lists Control Bit 4.

Table 2.13: CONTROL BIT 4

7	6	5	4	3	2	1	0
CBIT 32	CBIT 31	CBIT 30	CBIT 29	CBIT 28	CBIT 27	CBIT 26	CBIT 25

Table 2.14 lists Control Bit 5.

Table 2.14: CONTROL BIT 5

7	6	5	4	3	2	1	0
CBIT 40	CBIT 39	CBIT 38	CBIT 37	CBIT 36	CBIT 35	CBIT 34	CBIT 33

User-Defined SCM

The DSCM can be replaced with a user-defined SCM. To remove the DSCM, shut down power to the test head, then lift the DSCM. Two handles are attached to the DSCM.

Pin Electronics Card HF (PECHF)

The PECHF provides sixteen test channels of programmable level pulse drivers, dual level comparators, and bridge-type programmable loads to the test pin. Each channel has a pair of transmission clamps to correctly terminate devices that are mismatched to the DUT Interface Board (DIB) characteristic impedance.

All of these functions are independently controlled for each test pin. The sixteen test channels can function as 16 independent single-ended channels, or as 8 pairs of differential-ended channels.

Each test channel has a low power per Pin Parametric Measurement Unit (PPMU) that can force a voltage, and can independently measure voltage and current on each pin. This measurement can be for low level measurements, or for DC parametric measurements. The signals received through PPMUs are multiplexed to one 16 bit analog-to-digital converter.

Jumpers are placed on the boards as board identification numbers, which are read by an on-board register.

If an overtemperature occurs (temperature of PECHF is excessive), an interrupt that is generated is delivered to the tester mainframe.

NOTE This document describes the functions of the PECHF board. For detailed information on the operation of testing devices, refer to the online manual, *Digital Subsystem Hardware*.

Test Channel Functions

PECHF test channels can drive signals, compare DUT response, clamp transmissions, and perform parametric measurement.

Figure 2.10 on page 2-30 shows a block diagram of the test channel functions.

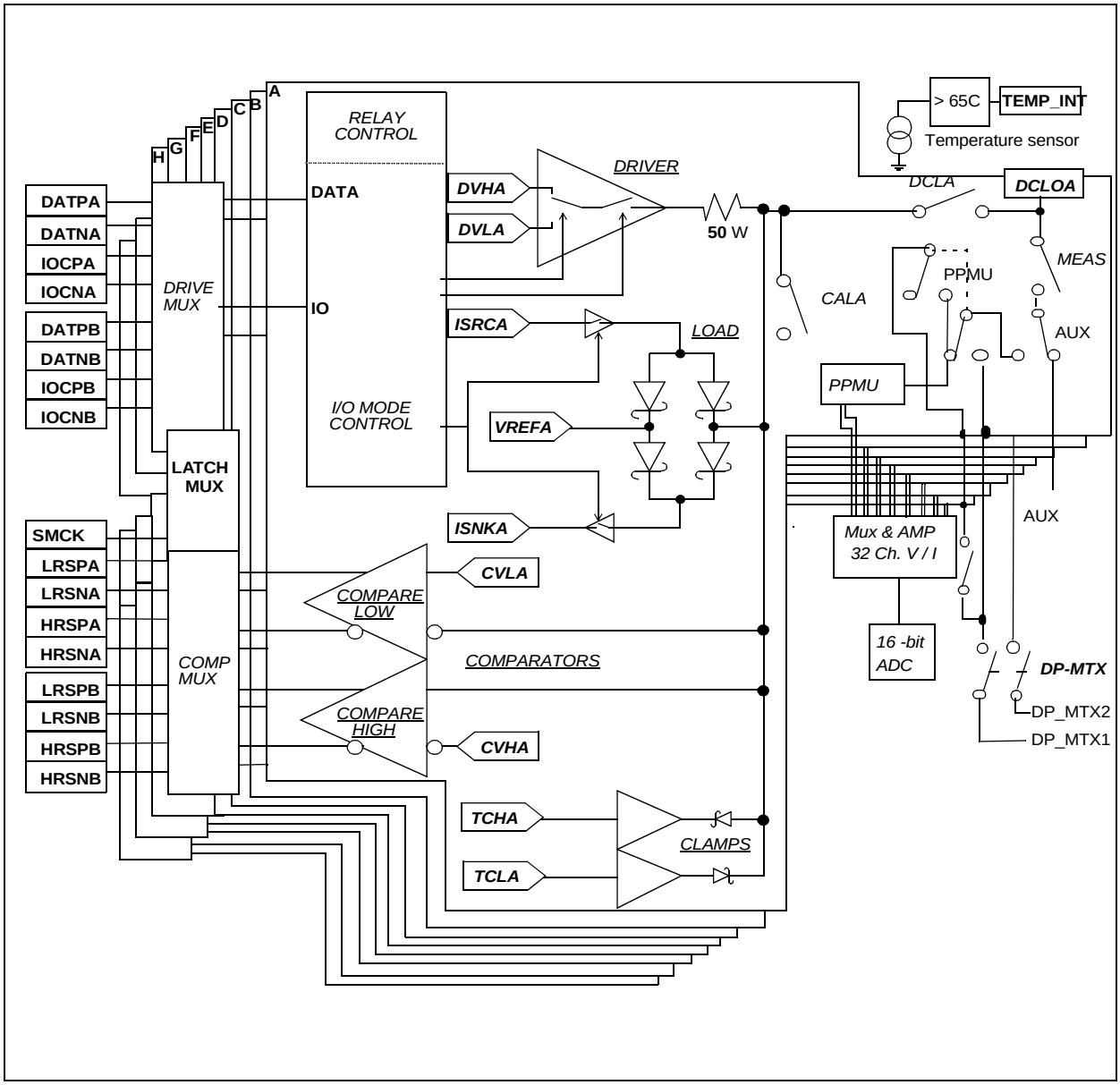

Figure 2.10: PECHF Test Channels, Block Diagram

Regarding Figure 2.10:

- Each layer represents one channel.
- One 16-bit ADC supports all 16 channels: The selected channel signal is delivered to the ADC through the multiplexer.
- Only eight of the 16 channels are illustrated.

Signal Drivers

Signal Drivers deliver the test pattern to the test pin. The drivers can function separately for single-ended signals, or in pairs for differential output. To deliver high speed waveforms at accelerated rates, data and I/O signals are exclusive-or'd (XOR).

Various modes of operation are available.

High-Speed Clock Mode. To achieve narrower pulse widths and higher clock rates than are available from the tester mainframe, the data and I/O signals of a pin channel are XOR'd.

NOTE When the IO signal is used as data, the programmed test channel is drive only: Responses from the DUT cannot be received.

Multiplex Mode / Differential Drive Mode. A pair of test channels can be programmed to drive two DUT pins with a 100-ohm differential-ended signal, or wired together and used as a single-ended 50-ohm driver. Pairs of channels are processed through one integrated circuit, PEHB2, and are driven by the same data: The propagation delays are minimal.

Multiplex mode is independent of the pin modes. It can be used with any combination of pin modes on the pair of channels.

Comparators

Comparators can be programmed to operate in either transparent mode, or in latch mode.

- Transparent mode: the comparator output constantly responds to the input.
- Latch mode: The comparator output is held (latched) until the next trigger.

The comparators can also be programmed to function with either single-ended signals or differential signals.

- Single-ended: Test channels are separate.
- Differential: Adjacent test channels function in pairs, e.g., channel A and channel B (refer to Figure 2.10, PECHF Test Channels, Block Diagram, on page 2-30).

Differential Compare Mode: Example. The differential compare mode tests differential outputs as a window comparator. To program this mode, the following information is required.

- The low offset voltage (VoffL)
- The high offset voltage (VoffH)
- The expected crossing voltage, within one Volt (Vexp)

Figure 2.11 illustrates a use of the window comparators on a single-ended signal, and a differential signal.

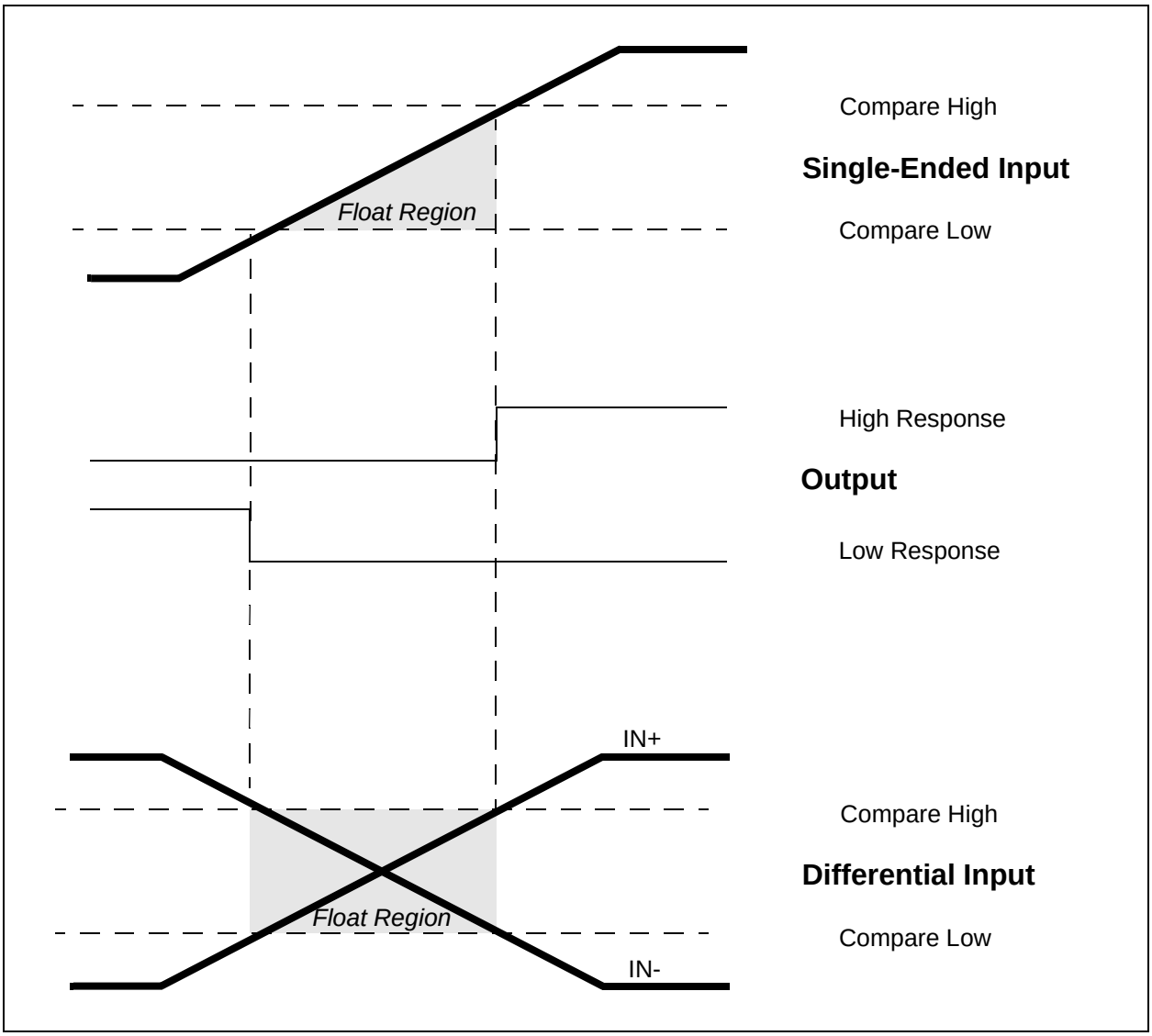

Figure 2.11: Window Comparators

In this illustrated example, test channel A is tied to the positive signal. If test channel B were tied to the positive signal the compare references would be reversed. The steps of this setup follow:

1. The comparator is connected to a programmable DC offset. The inputs of the DC offset are tied to the two test channels that were selected (programmed).

2. The low compare threshold is set to (InP - InN) - Low Offset.

3. The high comparator is set to (InP - InN) + High Offset.

4. Low Offset and High Offset are independent of each other. If an exact crossing point is necessary set either offset, or both offsets, to 0V.

5. Compare Voltage High on test channel A (CVHA) is programmed to Vexp + VoffH / 2.

6. On channel B, program CVHB for Vexp - VoffH / 2.

7. Program CVLA forVexp + VoffL / 2

8. Program CVLB for Vexp - VoffL / 2.

Compare Mux Mode. Compare Mux Mode delivers the data from the output of one test channel's comparator to the output of the other test channel's outputs. Setting bit CMUXA in the multiplex mode register sends test channel A comparator output out pin channel B; CMUXB sends pin channel B to pin channel A.

NOTE Setting both bits (CMUXA and CMUXB) reverses the comparator outputs.

Special Comparator Modes

The following modes can be used for testing high speed data.

High Speed Data Strobe Mode. Pairs of pins may be independently operated in this mode to enable multi-pass sampling of high speed data.

In High Speed Data Strobe Mode, the I/O line from the even numbered channels (A, C, E, G, J, L, N, Q) is used to strobe the receive comparators, for the respective pair of pins: I/O A strobes A and B, I/O C strobes C and D, etc.

Wideband Sampler Mode. In Wideband Same mode, a common sample clock input that is fed to the board can be routed to any pair of pin channels to strobe incoming or outgoing data. The important difference between Wideband Sampler Mode and High Speed Data Strobe Mode is that a high quality low jitter timing vernier can be used to trigger the sample: WBS permits the I/O line to function as normal.

Any number of pin pairs can be configured independently, which enables them to perform a waveform capture/Wide Band Sample function when driven by an external board.

Programmable Loads

The level of current load is programmable.

Load On Mode. The programmable loads are always on, the driver high/low function follows the data input and the driver on/off function follows the I/O input.

NOTE This mode is not often used in device testing; the programmable load current offsets the driver voltage.

Load Off Mode. The programmable loads are always off, the driver high/low function follows the data input and the driver on/off function follows the I/O input.

This mode is typically used with bidirectional DUT pins that do not require resistive termination or current source pull-up, or when either comparator bandwidth or off-state leakage is critical.

NOTE Programming the programmable loads to 0mA is not equivalent to *Load Off Mode.*

Transmission Clamps

Transmission clamps are connected to each test pin. The purpose is to protect the PECHF from current overload should a DUT fail.

If an overload occurs (current > 25mA), all PECHF relays are opened, and an interrupt is generated that is delivered to the tester mainframe.

PPMU

A Per Pin Parametric Measurement Unit (PPMU) is provided to each test channel for DC parametric measurement, or to force voltage. A PPMU is routed to the test pin by selecting the PPMU and MEAS relays. When selected, PPMU measurements are stored in memory.

DC Parametric Measurement. The PPMU measurement outputs are multiplexed to the 16-bit Analog-Digital Converter (ADC). Addresses delivered to the ADC Control Register select which PPMU measurement is delivered to the ADC.

The sense current is obtained by two buffer amplifiers monitoring the voltage drop across a series sense resistor. The output of these buffers are fed to a differential amplifier, which generates a voltage that is proportional to current. The non-inverting input of the differential amplifier is also fed to a buffer amplifier input which is used to give feedback control of the force.

Each PPMU has a total of eight ranges of current gain, and two ranges of voltage gain. These ranges of gain provide the necessary resolution for measurements. Refer to Figure 2.12, PPMU Measurement, on page 2-36 for a block diagram.

Voltage Measurement. The selected voltage sense buffer output is multiplexed to the 16-bit Analog-to-Digital converter (ADC). The results of the ADC are delivered to the tester mainframe.

Current Measurement. The selected current sense buffer output is multiplexed to the 16-bit ADC. The results of the ADC are delivered to the tester mainframe.

Sequencer. The Sequencer mode, also known as PPMU Auto-Mode, stores the selected PPMU measurements in memory. A selected PPMU measurements is converted to digital data (processed through a DAC), which is then stored in a PECHF memory register.

Force Voltage Mode. In Force Voltage mode, the 13 bit D/A sets the force voltage through the force operational amplifier non-inverting input. The voltage sense buffer output is fed back to the force operational amplifier inverting input, which gives feedback control to the operational amplifier.

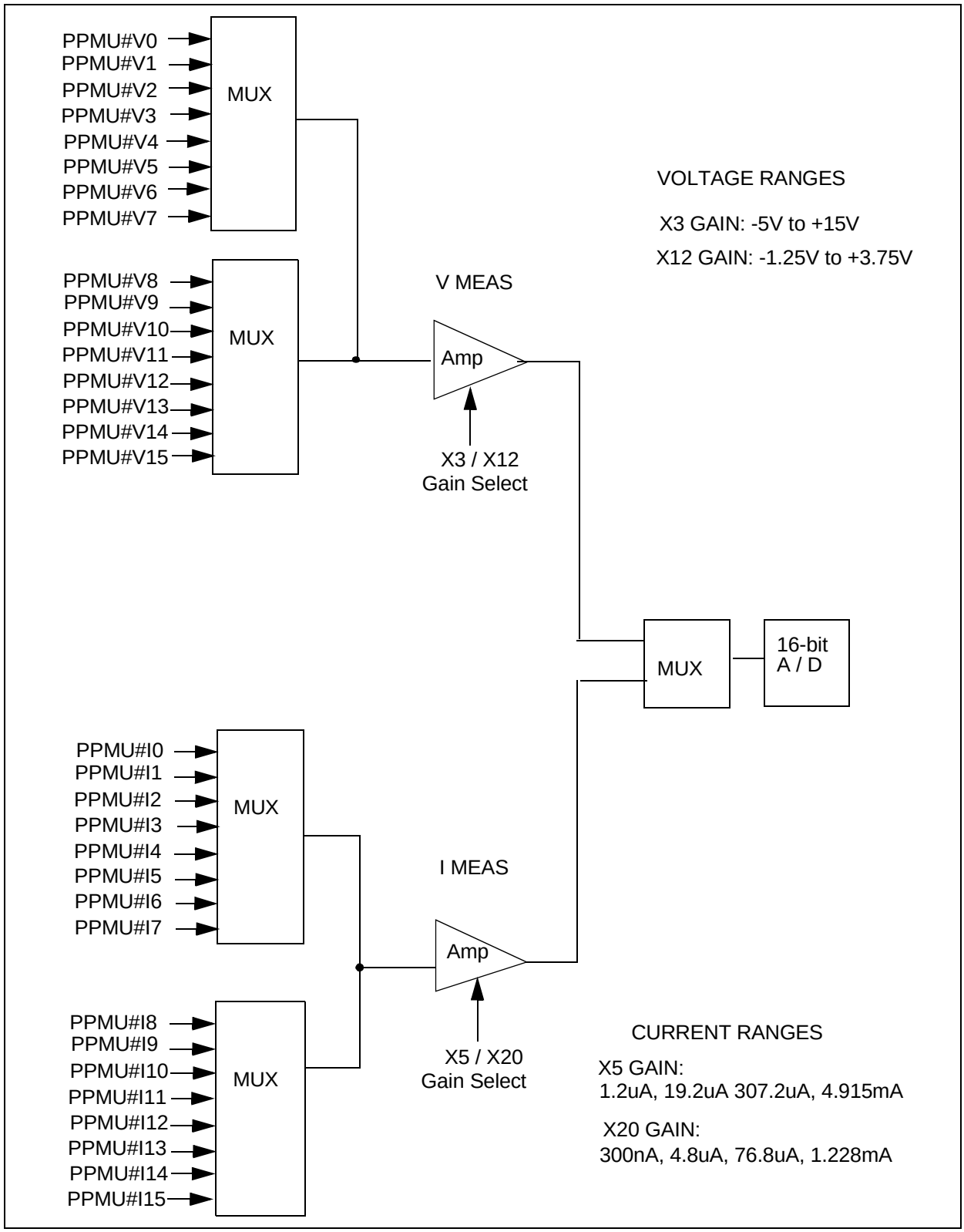

Figure 2.12: PPMU Measurement

Relays: Function Selection

Test channel functions are selected through relays.

Test Pin Relays. There are three relays per test pin: DCL, MEAS, and PPMU. These allow either Pin Electronic Hybrid (PEHB, a custom high-speed interface device), PPMU or a Central Analog Resource to be connected to the device under test (DUT) pin.

- DCL: The DCL relay connects the pin channel to the MEAS relay and the DUT. There is one DCL relay per test pin.
- MEAS: The MEAS relay connects the DUT node to the PPMU relay. This provides the low capacitance isolation for the signal path when no DC measurements are used. There is one MEAS relay per test pin.
- PPMU: The PPMU relay can connect either the PPMU or the APIN Bus to the MEAS relay input. There is one PPMU relay per test pin.

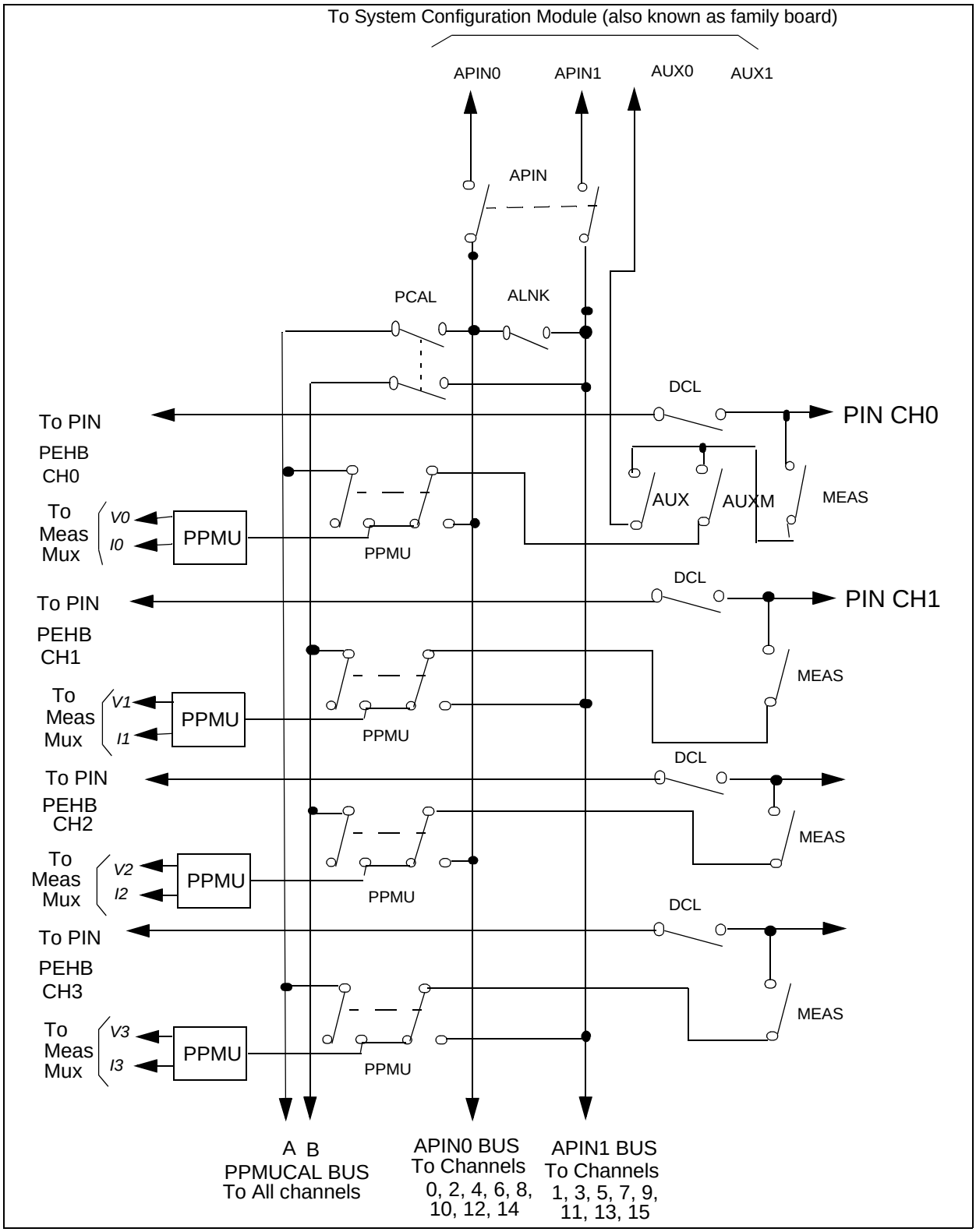

Figure 2.13: DUT Pin Relays

PECHF Board Relays. Following are the functions of the PECHF board relays.

- PCAL: The PPCAL relay connects the PPMU Bus to the Measure Bus. This enables the calibration of each PPMU via the Measure Bus to the CTMU (Central Timing Measurement Unit).
- APIN: The APIN Relay connects the boards two APIN Busses to the System Configuration Module (SCM, also known as family board).
- ALNK: The ALNK relay links the two APIN Busses together when energized.
- AUX: The AUX relay Connects a high speed input to CHA MEAS relay.

Pin Modes

The PECHF has a total of 96 possible pin modes. The PECHF receives two high-speed control signals from the timing generators: Data and I/O. These two signals control the data high/low signal, the driver on/off signal, and the programmable load on/off signal.

The low-speed pin modes determine how the two input signals are used to control the three PECHF functions.

Parallel Interface

The PECHF board is controlled through the parallel bus.

Table 2.15: Parallel Bus Signals

Signal	Function
ADDR	These lines control to which pin card slot and which register on the board the data is written.
DATA	This is a bidirectional 16-bit wide parallel data bus. The data rate is 4M word per second.
STB	WRITE: The rising edge of STB latches data into register READ: When STB is low, output data is enabled (for reading.
W	This signal enables data to be transferred to the FPGA when low.
R	This signal enables data to be transferred from the FPGA when low.
APW	Regardless of pin or slot address, this active high signal enables data to be transferred to the card when high.
RST	This sets all registers on PECHF to logic 0 and overrides the busy signal. All DACs are set to their mid-point.
SEQ	This pulse, in combination with a dummy FPGA2 write, enables the PPMU sequencer (minimum pulse duration = 10us after BUSY bus has been asserted). Once this has been asserted BUSY is held low until the sequence is complete. All control lines other than RST will be ignored during a sequence. SEQ MUST be set low again before the sequence can be completed.
BUSY	This goes low during either an A / D conversion or SEQ Note that during an A / D conversion control functions for the board are accepted while during a sequence they are ignored but either event drives BUSY low.
THINT	This is normally high Z and is active low when a temperature interrupt is generated.
INT	This is normally high Z and is active low when an interrupt is generated.

Write Cycle. During the write cycle, W is low, R is high. The fourteen parallel address bits are fed to the address decoder. If the slot portion of the parallel address agrees with the hard-wired slot value, then the rest of the address is decoded to determine to which register the data will be written. The data is then latched by STB.

Read Cycle. During the read cycle, R is low, W is high. The address is set up, then after the settling time, the strobe is set low. In read mode, the strobe functions as an output enable: Addressed register data is written to the data bus.

Test Head Interrupt. The Test Head Interrupt (THINT) signal of each PECHF is connected to the same receiver on the Test Head Bus Driver (THBDHF) board. On each PECHF, this signal is process through an open collector drive: Any PECHF can pull this line low to generate a test head interrupt which is delivered to the tester mainframe.

The information of the cause of the interrupt is available in PECHF registers, which are read by the tester mainframe. For detailed information about registers, refer to the Register Data Base Utility (RDBU).

Bus Definition. There are 4 slot address lines. Addressing is split into groups of 256 pins. Each 256-pin driver module has an enable line from the THBDHF, which permits individual pin card selection or all pin write.

Registers

Following is a description of four PECHF registers. For detailed information on all registers, refer to the Register Data Base Utility (RDBU).

Serial Number Register. The serial number register reads the serial number jumpers that identify the PECHF board. There is one serial number register per board.

Board Status Register. There is one board status register per PECHF board. The register processes interrupts and ADC activity.

Overload Interrupt Register. An interrupt occurs if transmission clamps are overloaded: subjected to excess current.

Reading the overload interrupt register does not clear either an overload interrupt or a temperature interrupt. The only method to clear an interrupt is to assert the PECHF reset input

Register Reset. The THBDHF automatically issues the clear command on power-up. Register Reset also occurs when the PECHF reset line is asserted.

When Register Reset is executed, all sixteen Pin Function Registers are cleared to '0', all relays are opened, all DACs are reset to mid-scale, and all latched interrupts are cleared. However, clear command does not clear an interrupt if the interrupt condition is still present.

PECHF I/O

The PECHF interfaces the following signals:

- High speed I/O signals
- DSCM signals

High Speed Interface. Signals transmit through PECHF connectors P2 and P1.

Table 2.16 shows the high speed interface at P2.

Table 2.16: High Speed Signals Connector P2

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
1 : FARMGND	41 : IOCPC	81 : HRSPG	121 : FARMGND	161 : HRSNR
2 : FARMGND	42 : IOCPB	82 : HRSPF	122 : FARMGND	162 : HRSNN
3 : LRSPD	43 : FARMGND	83 : HRSNG	123 : DATNJ	163 : FARMGND
4 : LRSPA	44 : FARMGND	84 : HRSNG	124 : DATNJ	164 : FARMGND
5 : LRSND	45 : DATNC	85 : FARMGND	125 : DATPM	165 : IOCNR
6 : LRSNA	46 : DATNB	86 : FARMGND	126 : DATPJ	166 : IOCNN
7 : FARMGND	47 : DATPC	87 : IOCNG	127 : FARMGND	167 : IOCPR
8 : FARMGND	48 : DATPB	88 : IOCNF	128 : FARMGND	168 : IOCPN
9 : HRSPD	49 : FARMGND	89 : IOCPG	129 : LRSPL	169 : IOCPN
10 : HRSPA	50 : FARMGND	90 : IOCPF	130 : LRSPK	170 : FARMGND
11 : HRSND	51 : LRSPH	91 : FARMGND	131 : LRSNL	171 : DATNR
12 : HRSNA	52 : LRSPE	92 : FARMGND	132 : LRSNK	172 : DATNN
13 : FARMGND	53 : LRSHG	93 : DATNG	133 : FARMGND	173 : DATPR
14 : FARMGND	54 : LRSNE	94 : DATNF	134 : FARMGND	174 : DATPN
15 : IOCND	55 : FARMGND	95 : DATPG	135 : HRSPL	175 : FARMGND
16 : IOCNA	56 : FARMGND	96 : DATPF	136 : HRSPK	176 : FARMGND
17 : IOCPD	57 : HRSPH	97 : FARMGND	137 : HRSNL	177 : LRSPQ

Table 2.16: High Speed Signals Connector P2 (Continued)

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
18 : IOCPA	58 : HRSPE	98 : FARMGND	138 : HRSNK	178 : LRLSPP
19 : FARMGND	59 : HRSNH	99 : FARMGND	139 : FARMGND	179 : LRSNQ
20 : FARMGND	60 : HRSNE	100 : FARMGND	140 : FARMGND	180 : LRSNP
21 : DATND	61 : FARMGND	101 : FARMGND	141 : IOCNL	181 : FARMGND
22 : DATNA	62 : FARMGND	102 FARMGND	142 : IOCNK	182 : FARMGND
23 : DATPD	63 : IOCNG	103 : FARMGND	143 : IOCPL	183 : HRSPQ
24 : DATPA	64 : IOCNE	10R : FARMGND	144 : IOCPK	184 : HRSPP
25 : FARMGND	65 : IOCPH	105 : LRSPM	145 : FARMGND	185 : HRSNQ
26 : FARMGND	66 :IOCPE	106 : LRSPJ	146 : FARMGND	186 : HRSNP
27 : LRSPC	67 : FARMGND	107 LRSNM	145 : DATNL	187 : FARMGND
28 : LRSPB	68 : FARMGND	108 : LRSNJ	148 : DATNK	188 : FARMGND
29 : LRSNC	69 : DATNH	109 : FARMGND	149 : DATPL	189 : IOCNQ
30 : LRSNB	70 : DATNE	110 : FARMGND	150 : DATPK	190 : IOCNP
31 : FARMGND	71 : DATPH	111 : HRSPM	151 : FARMGND	191 : IOCPQ
32 : FARMGND	72 : DATPE	112 : HRSPJ	152 : FARMGND	192 : IOCPP
33 : HRSPC	U3 : FARMGND	113 : HRSNM	153 : LRSPR	193 : FARMGND
34 : HRSPB	74 : FARMNGND	114 : HRSNJ	154 : LRSPN	194 : FARMGND
35 : HRSNC	75 : LRSPG	115 : FARMGND	155 LRSNG	195 : DATNQ
36 : HRSNG	65 : LRSPF	116 : FARMGND	156 : LRSNN	196 : DATNP
37 : FARMGND	77 : LRSNG	117 : IOCNM	157 : FARMGND	197 : DATPQ
38 : FARMGND	78 : LRSNG	118 : IOCNG	158 : FARMGND	198 ; DATPP
39 : IOCNC	79 : FARMGND	119 : IOCPM	159 : HRSPR	199 : FARMGND
40 : IOCNG	80 : FARMGND	120 : IOCPJ	160 : HRSPN	200 : FARMGND

Table 2.17 shows the high Speed Interface at J3.

Table 2.17: Pin-Out for High Speed Interface J3

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
A1: HRSPJ	B1 : HRSNJ	C1 : GND	D1 : LRSPJ	E1 : LRSNJ
A2 : DATPJ	B2 : DATNJ	C2 : GND	D2 : IOCPJ	E2 : IOCNJ
A3: GND	B3 : GND	C3 : GND	D3 : GND	E3: GND
A4 : HRSPK	B4 : HRSNK	C4 : GND	D4 : LRSPK	D4 : LRSNK
A5 : DATPK	B5 : DATNK	C5 : GND	D5 ; IOCPK	E5 : IOCNK
A6 : GND	B6 : GND	C6 : GND	D6 : BND	E6 : GND
A7 : HRSPL	B7 : HRSNL	C7 : GND	D7 : LRSPL	E7 : LRSNL
A8 : DATPL	B8 : DATNL	C8 : GND	D8 : IOCPL	E8 : IOCNL
A9 : GND	B9 : GND	C9 : GND	D9 : GND	E9 : GND
A10 : HRSPM	B10 : HRSNM	C10 : GND	D10 : LRSPM	E10 : LRSNM
A11 : DATPM	B11 : DATNM	C11 : GND	D11 : IOCPM	E11 : IOCNM
A15 : HRSPN	B15 : HRSNN	C15 : GND	D15 : LRSPN	E15 : LRSNN

DSCM Signal I/O

Table 2.18 shows the default connections from the PECHF to the Split Interface Plate through the DSCM.

Table 2.18: DSCM Connector P1

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
1 : AUXG	2 : AUX	3 : HSCKA	4 : APIN2GUA
5 : HSCKG	6 : APIN1GUA	7 : HSCKB	8 : APIN1
9 : THRG	10 : APIN2	11 :GND	12 : GND
13 : GND	14 : GND	15 : VC20	16 : VC20
17 : VC15	18 : VC15	19 : VC15	20 : VC15
21 : GND	22 : GND	23 : VC10	24 : VC10
25 : VC10	26 : VC10	27 : GND	28 : GND
29 : GND	30 : GND	31 : VC5	32 : VC5
33 : VC5	34 : VC5	35 : GND	36 : GND
37 : GND	38 : GND	39 : GND	40 : GND

Table 2.18: DSCM Connector P1 (Continued)

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
41 : VE5	42 : VE5	43 : VE5	44 : VE5
45 : VE5	46 : VE5	47 : VE5	48 : VE5
49 : VE5	50 : VE5	51 : GND	52 : GND
53 : GND	54 : GND	55 : VE10	56 : VE10
57 : VE10	58 : VE10	59 : VE15	60 : GND
61 : VE15	62 : GND	63 : SEQ	64 : RESET
65 : SEQG	66 : RESETG	67 : READG	68 : STROBEG
69 : READ	70 : STROBE	71 : APWR	72 : WRITE
73 : APWRG	74 : WRITEG	75 : SLTAD3	76 : SLTAD1
77 : SLTAD2	78 : SLTAD0	79 : SLTGND	80 : ADDRG
81 : ADDRG	82 : ADDRG	83 : ADDR13	84 : ADDR6
85 : ADDR12	86 : ADDR5	87 : ADDR11	88 : ADDR4
89 : ADDR10	90 : ADDR3	91 : ADDR9	92 : ADDR2
93 : ADDR8	94 : ADDR1	95 L: ADDR7	96 : ADDR0
97 : ADDRG	98 : ADDRG	99 : ADDRG	100 : ADDRG
101 : DATAG	102 : DATAG	103 : DATAG	104 : DATAG
105 : DATA15	106 : DATA7	107 : DATA14	108 : DATA6
109 : DATA13	110 : DATA5	111 : DATA12	112 : DATA4
113 : DATA11	114 : DATA3	115 : DATA10	116 : DATA2
117 : DATA9	118 : DATA1	119 : DATA8	120 : DATA0
121 : DATAG	122 : DATAG	123 : DATAG	124 : DATAG
125 : THINT	126 : TEMPINT	127 : INTG	128 : LEAKD
129 : BUSYG	130 : LPBK	131: BUSY	132 : LPBK

Thermal Management

Thermal management is controlled with a closed loop cooling system. When properly installed in the test head, the copper plates on the PECHF boards contact the Membrane Cooling Modules (MCM) that circulate water. This method transfers heat from the PECHF to the cooling media.

Test Head Bus Driver (THBDHF)

The Test Head Bus Driver HF (THBDHF) is a digital test head bus driver that relays communications between the mainframe tester and the test head.

The THBDHF interfaces to the 64 pin electronics cards (PECs) in quadrants, groups of 16, through Test Head Buffer cards (THBUF). There are four THBUFs attached to the THBDHF. Each THBUF buffers signals to / from 16 PECs: 256 test channels. The THBUF communicates to the PECs through the test head digital backplane.

A THBUF is connected to the THBDHF through a flexible flat ribbon cable, and an adapter card, THBCN. The THBN has no electronics; it is simply an interface connector.

One THBDHF is required per test head, and is located in the analog crate (card cage) of the Fusion HF test head. Refer to Figure 2.9, Fusion HF Test Head Analog Backplane, on page 2-17.

Serial Communication

The serial data bus can transport data at 622Mbits per second. When receiving data from the mainframe, THBDHF converts streams of serial data to parallel words. Delivering data to mainframe, parallel words are converted to serial bits. The serial data is encoded into a 16-bit parallel data words with 14-bit addresses. Refer to Figure 2.14, THBDHF, Block Diagram, on page 2-48.

As the serial data port is asynchronous, the information received by the THBDHF from the tester mainframe, is echoed back to the mainframe. Looping back the data indicates when the THBDHF is ready to process another transaction, and enables the mainframe to check for errors.

When an interrupt is delivered to the tester mainframe, the THBDHF suspends the current communication, if any, to send the interrupt control word. Immediately after the interrupt has been sent the reception or transmission of data continues from where it left off.

Addressing PEC

Commands can be delivered to specific PECs by address. Separated into quadrants of 16 boards, there are 16 addresses: 0 - 15. These addresses are coded into 4 bits of the backplane.

There is also an all-pin-write line on the backplane, which informs all PECs to accept the data on the bus.

PECHF Status

The THBDHF also buffers the interrupt lines from the digital pin cards to the mainframe. Information of the state of the delivered interrupts, and the identification of which PECs delivered the interrupts, are stored in registers that are accessible to the mainframe.

Test Head Buffer (THBUF)

The function of the THBUF is strictly to buffer signals. The THBDHF delivers four copies of the encoded parallel data word and address data to the four THBUFs. Each copy is delivered to the four groups of PECs through the THBUF buffer boards.

Test Head Buffer Connector (THBCN)

The THBCN board is a transition card that plugs onto the THBDHF 200 pin I/O connector and carries the signals to four ribbon cables, one for each THBUF. The THBCN has no active components or power requirements.

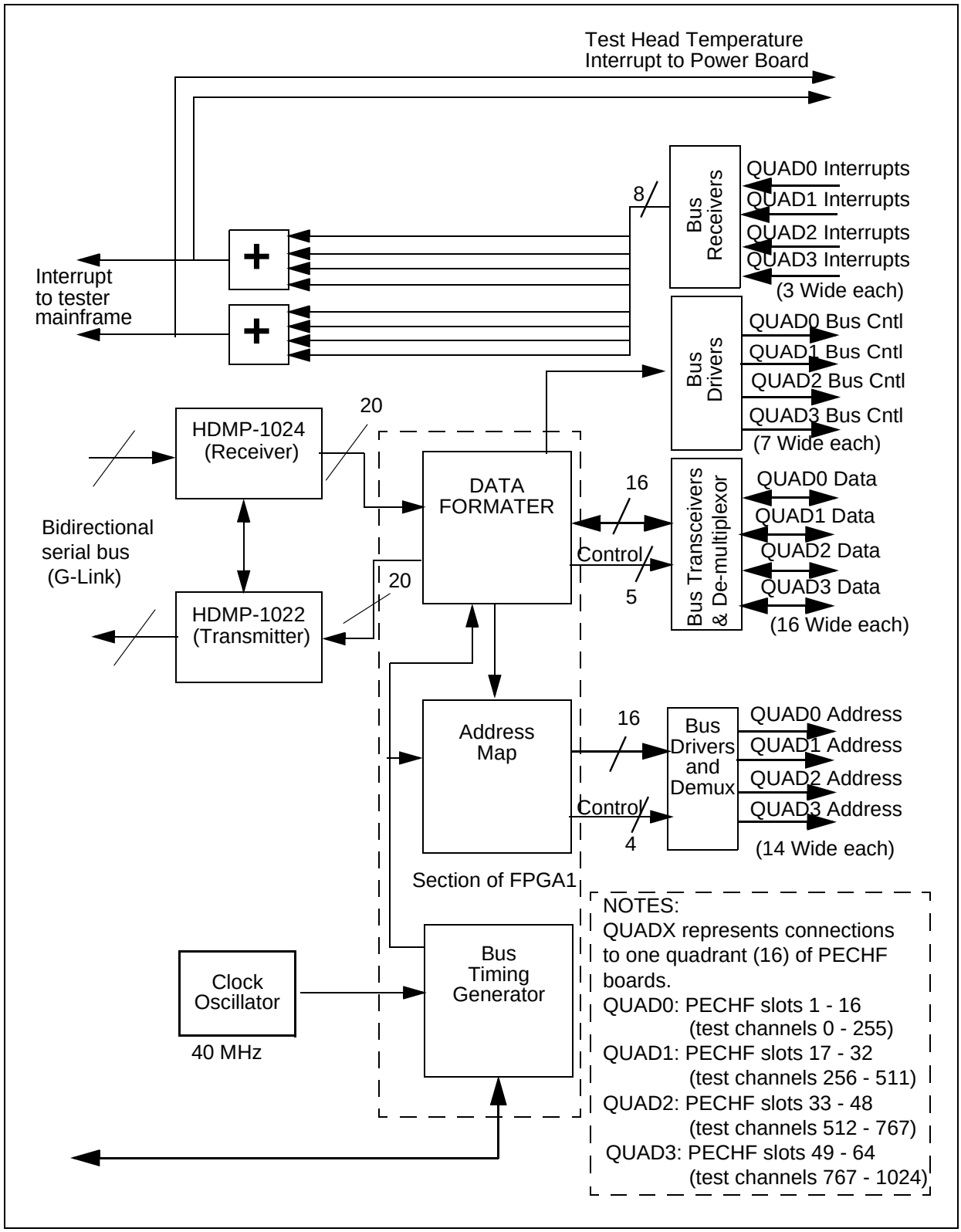

Figure 2.14: THBDHF, Block Diagram

I/O Signals

The following tables list the pins of the I/O signals.

Table 2.19 shows the data bus signals

Table 2.19: Test Head Data Bus Signals

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
1 : Q0 Sequence	2: Q0 Reset*	101 : Q2 Sequence	102 : Q2 Reset*
3 : +5V	4 : Ground	103 : +5V	104 : Ground
5 : Q0 Read*	6 : Q0 Write*	105 : Q2 Read*	106 : Q2 Write*
7 : Q0 Enable*	8 : Ground	107 : Q2 Enable*	108 : Ground
9 : All Pin Write	10 : Q0 Strobe	109 : All Pin Write	110 : Q2 Strobe
11 : Ground	12 : Ground	111 : Ground	112 : Ground
13 : Q0 Adr[13]	14 : Q0 Adr[12]	113 : Q2 Adr[13]	114 : Q2 Adr[12]
15 : Q0 Adr[11]	16 : Q0 Adr[10]	115 : Q2 Adr[11]	116 : Q2 Adr[10]
17 : Q0 Adr[9]	18 : Q0 Adr[8]	117 : Q2 Adr[9]	118 : Q2 Adr[8]
19 : Q0 Adr[7]	20 : Q0 Adr[6]	119 : Q2 Adr[7]	120 : Q2 Adr[6]
21 : Q0 Adr[5]	22 : Q0 Adr[4]	121 : Q2 Adr[5]	122 : Q2 Adr[4]
23 : Q0 Adr[3]	24 : Q0 Adr[2]	123 : Q2 Adr[3]	124 : Q2 Adr[2]
25 : Q0 Adr[1]	26 : Q0 Adr[0]	125 : Q2 Adr[1]	126 : Q2 Adr[0]
27 : Ground	28 : Ground	127 : Ground	128 : Ground
29 : Q0 Data[15]	30 : Q0 Data[14]	129 : Q2 Data[15]	130 : Q2 Data[14]
31 : Q0 Data[13]	32 : Q0 Data[12]	131 : Q2 Data[13]	132 : Q0 Data[12]
33 : Q0 Data[11]	34 : Q0 Data[10]	133 : Q2 Data[11]	134 : Q2 Data[10]
35 : Q0 Data[9]	36 : Q0 Data[8]	135 : Q2 Data[9]	136 : Q2 Data[8]
37 : Q0 Data[7]	38 : Q0 Data[6]	137 : Q2 Data[7]	138 : Q2 Data[6]
39 : Q0 Data[5]	40 : Q0 Data[4]	139 : Q2 Data[5]	140 : Q2 Data[4]
41 : Q0 Data[3]	42 : Q0 Data[2]	141 : Q2 Data[3]	142 : Q2 Data[2]
43 : Q0 Data[1]	44 : Q0 Data[0]	143 : Q2 Data[1]	144 : Q2 Data[0]
45 : Ground	46 : +5V	145 : Ground	146 : +5V
47 : Q0 Interrupt*	48 : Q0 Temperature Interrupt*	147 : Q2 Interrupt	148 : Q2 Temperature Interrupt
49 : Q0 Busy*	50 : Ground	149 : Q2 Busy*	150 : Ground

Table 2.19: Test Head Data Bus Signals (Continued)

Pin No. : Signal	Pin No. : Signal	Pin No. : Signal	Pin No. : Signal
51 : Q1 Sequence	51 : Q1 Reset*	151 : Q3 Sequence	152 : Q3 Reset*
53 : +5V	54 : Ground	153 : +5V	154 : Ground
55 : Q1 Read*	56 : Q1 Write*	155 : Q3 Read*	156 : Q3 Write*
57 : Q1 Enable*	58 : Ground	157 : Q3 Enable*	158 : Ground
59 : All Pin Write	60 : Q1 Strobe	159 : All Pin Write	160 : Q3 Strobe
61 : Ground	62 : Ground	161 : Ground	162 : Ground
63 : Q1 Adr[13]	64 : Q1 Adr[12]	163 : Q3 Adr[13]	164 : Q3 Adr[12]
65 : Q1 Adr[11]	66 : Q1 Adr[10]	Q3 165 : Adr[11]	166 : Q3 Adr[10]
67 : Q1 Adr[9]	68 : Q1 Adr[8]	167 : Q3 Adr[9]	168 : Q3 Adr[8]
68 : Q1 Adr[7]	70 : Q1 Adr[6]	169 : Q3 Adr[7]	170 : Q3 Adr[6]
71 : Q1 Adr[5]	72 : Q1 Adr[4]	171 : Q3 Adr[5]	172 : Q3 Adr[4]
73 : Q1 Adr[3]	74 : Q1 Adr[2]	173 : Q3 Adr[3]	174 : Q3 Adr[2]
75 : Q1 Adr[1]	76 : Q1 Adr[0]	175 : Q3 Adr[1]	176 : Q1 Adr[0]
77 : Ground	78 : Ground	177 : Ground	178 : Ground
79 : Q1 Data[15]	80 : Q1 Data[14]	179 : Q3 Data[15]	180 : Q3 Data[14]
81 : Q1 Data[13]	82 : Q1 Data[12]	180 : Q3 Data[13]	182 : Q3 Data[12]
83 : Q1 Data[11]	84 : Q1 Data[10]	183 : Q3 Data[11]	184 : Q3 Data[10]
85 : Q1 Data[9]	86 : Q1 Data[8]	185 : Q3 Data[9]	186 : Q3 Data[8]
87 : Q1 Data[7]	88 : Q1 Data[6]	187 : Q3 Data[7]	188 : Q3 Data[6]
89 : Q1 Data[5]	90 : Q1 Data[4]	189 : Q3 Data[5]	190 : Q3 Data[4]
91 : Q1 Data[3]	92 : Q1 Data[2]	191 : Q3 Data[3]	192 : Q3 Data[2]
93 : Q1 Data[1]	94 : Q1 Data[0]	193 : Q3 data[1]	194 : Q3 Data[0]
95 : Ground	96 : +5V	195 : Ground	196 : +5V
97 : Q1 Interrupt*	98 : Q1 Temperature Interrupt*	197 : Q3 Interrupt	198 : Q3 Temperature Interrupt
99 : Q1 Busy*	100 : Ground	199 : Q3 Busy*	200 : Ground

Table 2.20 shows the signals connected to the analog backplane.

Table 2.20: Analog Backplane Board ID and DC Power Signals

Pin No. : Signal	Pin No. : Signal
1 : EE_EN	2 : +5_EEPROM
3 : EE_CLK	4 : NC
5 : EE_DDATA	6 : +10V_THBD
7 : Ground	8 : Ground
9 : +5V_THBD	10 : +5V_THBD
11 : +5V_THBD	12 : +5V_THBD
13 : Ground	14 : Ground
15 : Ground	16 : Ground
17 : -5.2V_THBD	18 : -5.2V_THBD
19 : -5.2V_THBD	20 : -5.2V_THBD
21 : TEMP_HI*	22 : NC (No Connection)
23 : NC	24 : NC
25 : NC	26 : NC
27 : NC	28 : NC
29 : NC	30 : NC
31 : NC	32 : NC
33 : NC	34 : NC
35 : NC	36 : NC
37 : NC	38 : Nc
39 : NC	40 : NC
41 : NC	42 : NC
43 : NC	44 : NC
45 : NC	46 : NC
47 : NC	48 : NC
49 : NC	50 : NC

Table 2.21 shows the signals through the ZIF connector.

Table 2.21: Bottom 50 Pin ZIF Connector

Pin No. : Signal	Pin No. : Signal
1 : Ground	2 : NC
3 :Serial_In+	4 : NC
5 : Serial_In-	6 : NC
7 : Ground	8 : NC
9 : Ground	10 : NC
11 : Serial_Out+	12 : NC
13 : Serial_Out-	14 : NC
15 : Ground	16 : NC
17 : Ground	18 : NC
19 : Ana_Relay0	20 : Ana_Relay1
21 : Ana_Relay2	22 : Ana_Relay3
23 : Ground	24 : Ground
25 : TH_Interrupt	26 : TH_OT_Intrp
27 : Ground	28 : Ground
29 : NC	30 : NC
31 : NC	32 : NC
33 : NC	34 : NC
35 : NC	36 : NC
37 : NC	38 : NC
39 : NC	40 : NC
41 : LOOP_DIAG	42 : NC
43 : NC	44 : NC
45 : JTAG_TDI	46 : JTAG_TDO
47 : JTAG_TMS	48 : JTAG_TCK
49 : JTAG_TRST	50 : NC

Thermal Management

The THDBHF board is air cooled through forced air.

Test Head Buffer (THBUF)

Four Test Head Buffer modules are connected to the THBDHF, each of which connects to one quadrant (16) of the pin electronic cards in the test head.

I/O Signals. Table 2.22 shows the I/O signals to the PECHF boards.

Table 2.22: THBDHF Buffer Board to Test Head Connection

Pin No. : Signal	Pin No. : Signal
1 : SEQ0	2 : RESET0
3 : +5V_THBD	4 : Ground
5 : READ0	6 : WRITE0
7 : Ground	8 : Ground
9 : ALLPIN0	10 : STB0
11 : Ground	12: Ground
13 : ADDR0[13]	14 : ADDR0[12]
15 : ADDR0[11]	16 : ADDR0[10]
17 : ADDR0[9]	18 : ADDR0[8]
19 : ADDR0[7]	20 : ADDR0[6]
21 : ADDR0[5]	22 : ADDR0[4]
23 : ADDR0[3]	24 : ADDR0[2]
25 : ADDR0[1]	26 : ADDR0[0]
27 : Ground	28 : Ground
29 : DATA0[15]	30 : DATA0[14]
31 : DATA0[13]	32 : DATA0[12]
33 : DATA0[11]	34 : DATA0[10]
35 : DATA0[9]	36 : DATA0[8]
37 : DATA0[7]	38 : DATA0[6]
39 : DATA0[5]	40 : DATA0[4]
41 : DATA0[3]	42: DATA0[2]
43 : DATA0[1]	44 : DATA0[0]
45 : Ground	46 : +5V_THBD
47 : THINT0	48 : TEMPINT0

Table 2.22: THBDHF Buffer Board to Test Head Connection (Continued)

Pin No. : Signal	Pin No. : Signal
49 : BUSY0	50 : Ground

Thermal Management

The THBUF boards are air cooled through forced air.

HF Digital Backplane (HFDBP)

HFDBP is the HF Digital Backplane for the Fusion HF test head. It provides the communication bus and the control signals for all 64 16-pin, digital pin electronic cards. The HFDBP also has five HDI connectors that connect directly to the System Configuration Module (SCM, also known as family board). These connectors brings signals from the pin electronic cards (PEC), and from the mainframe to the SCM.

Figure 2.15, Digital Backplane Connectors, on page 2-55 shows an overview of the connectors of the digital backplane.

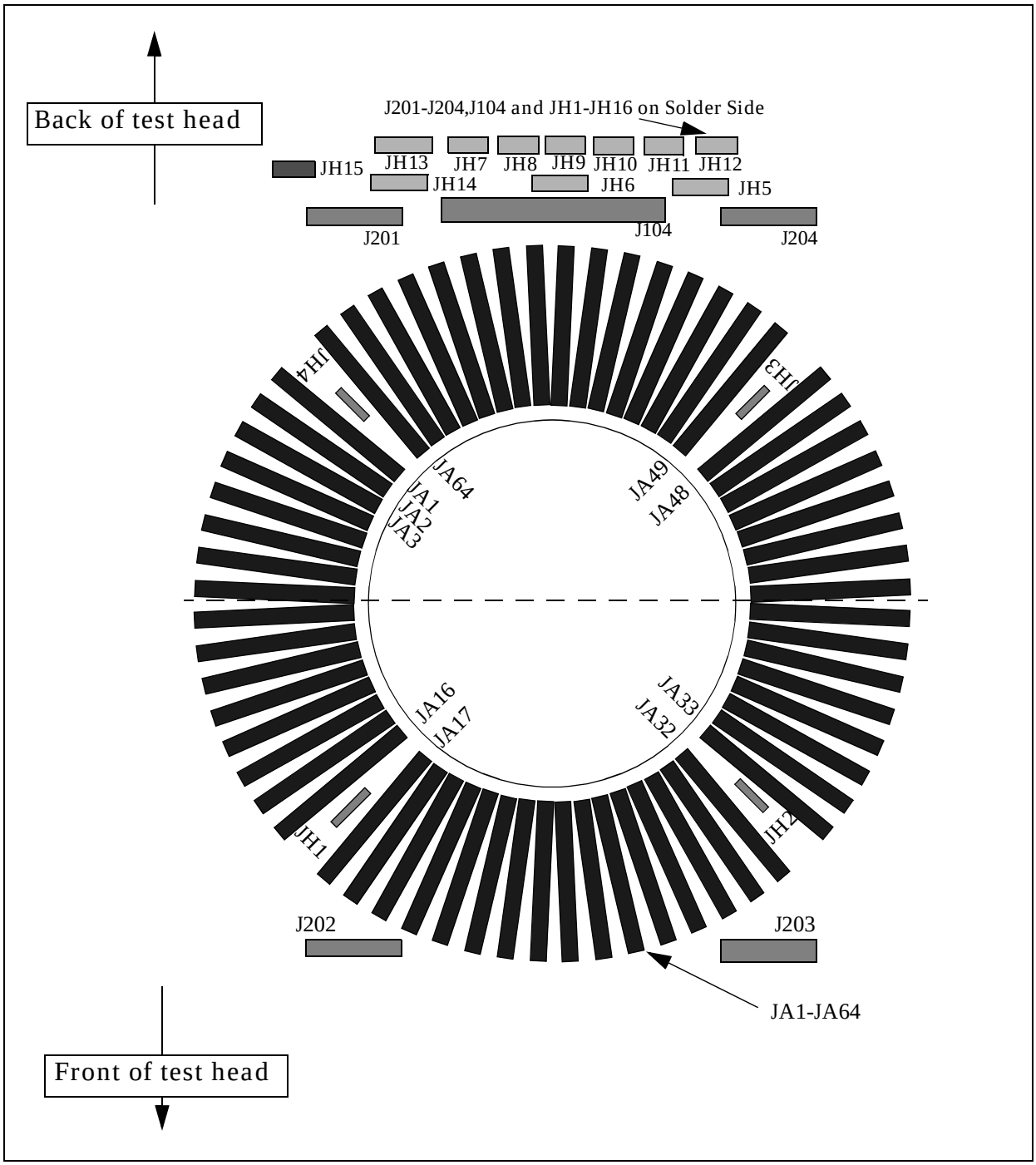

Figure 2.15: Digital Backplane Connectors

Mainframe Connectors

Table 2.23 on page 2-56 shows the connector assignments for signals to/from the tester mainframe. To see the layout of the connectors, refer to Figure 2.15 on page 2-55

Table 2.23: Mainframe Connector Assignments

Connector	Function	Connector type
J104	Family Board	HDI - 240 pin
J201	DPMTX 56-7	HDI - 100 pin
J202	DPMTX 8-23	HDI - 100 pin
J203	DPMTX 24-39	HDI - 100 pin
J204	DPMTX 40-55	HDI - 100 pin
JH1	THBD 0	2 x 25 pin, surface mount
JH2	THBD 1	2 x 25 pin, surface mount
JH3	THBD 2	2 x 25 pin, surface mount
JH4	THBD 3	2 x 25 pin, surface mount
JH5	CBIT 1-32	50 pin 2 row Header connector
JH6	CBIT 33-48	50 pin 2 row Header connector
JH7	DPS 1-2	16 pin 2 row Header connector
JH8	DPS 3-4	16 pin 2 row Header connector
JH9	DPS 5-6	16 pin 2 row Header connector
JH10	DPS 7-8	16 pin 2 row Header connector
JH11	DPS 9-10	16 pin 2 row Header connector
JH12	DPS 11-12	16 pin 2 row Header connector
JH13	MS	50 pin 2 row Header connector
JH14	Spare	50 pin 2 row header connector
JH15	Remote Power and Leak Sense	16 pin 2 row header connector
JH16	Board ID	16 pin 2 row header connector
JG1-64	HSCK	3 pin 1 row header connector

Digital Test Channels

Table Table 2.24 shows the group of digital pin test channels per backplane connector / PECHF board. To see the location of the connectors, refer to Figure 2.15 on page 2-55.

Table 2.24: Digital Pin Test Channels

Connector	Digital Pin Test Channel Group	Connector	Digital Pin Test Channel Group
JA1	0-15	JA33	128-143
JA2	512-527	JA34	640-655
JA3	256-271	JA35	384-399
JA4	768-783	JA36	896-911
JA5	16-31	JA37	144-159
JA6	528-543	JA38	656-671
JA7	272-287	JA39	400-415
JA8	784-799	JA40	912-927
JA9	32-47	JA41	160-175
JA10	544-559	JA42	672-687
JA11	288-303	JA43	416-431
JA12	800-815	JA44	928-943
JA13	48-63	JA45	176-191
JA14	560-575	JA46	688-703
JA15	304-319	JA47	432-447
JA16	816-831	JA48	944-959
JA17	64-79	JA49	192-207
JA18	576-591	JA50	704-719
JA19	320-335	JA51	448-463
JA20	832-847	JA52	960-975
JA21	80-95	JA53	208-223
JA22	592-607	JA54	720-735
JA23	336-351	JA55	464-479
JA24	848-863	JA56	976-991
JA25	96-111	JA57	224-239
JA26	608-623	JA58	736-751

Table 2.24: Digital Pin Test Channels (Continued)

Connector	Digital Pin Test Channel Group	Connector	Digital Pin Test Channel Group
JA27	352-367	JA59	480-495
JA28	864-879	JA60	992-1007
JA29	112-127	JA61	240-255
JA30	624-639	JA62	752-767
JA31	368-383	JA63	496-511
JA32	880-895	JA64	1008-1023

System Configuration Module, J104

Table 2.25 on page 2-58 lists the signals of J104, the HDI connector to the System Configuration Module (SCM).

Table 2.25: SCM Connector J104

Row A Pin #	Signal	Row B Pin #	Signal	Row C Pin #	Signal	Row D Pin #	Signal
1	GND	1	GND	1	GND	1	GND
2	GND	2	GND	2	GND	2	GND
3	CBIT(31)	3	CBIT(32)	3	CBIT(63)	3	CBIT(64)
4	CBIT(29)	4	CBIT(30)	4	CBIT(61)	4	CBIT(62)
5	CBIT(27)	5	CBIT(28)	5	CBIT(59)	5	CBIT(60)
6	CBIT(25)	6	CBIT(26)	6	CBIT(57)	6	CBIT(58)
7	CBIT(23)	7	CBIT(24)	7	CBIT(55)	7	CBIT(56)
8	CBIT(21)	8	CBIT(22)	8	CBIT(53)	8	CBIT(54)
9	CBIT(19)	9	CBIT(20)	9	CBIT(51)	9	CBIT(52)
10	CBIT(17)	10	CBIT(18)	10	CBIT(49)	10	CBIT(50)
11	GND	11	GND	11	GND	11	GND
12	GND	12	GND	12	GND	12	GND
13	CBIT(15)	13	CBIT(16)	13	CBIT(47)	13	CBIT(48)
14	CBIT(13)	14	CBIT(14)	14	CBIT(45)	14	CBIT(46)
15	CBIT(11)	15	CBIT(12)	15	CBIT(43)	15	CBIT(44)
16	CBIT(9)	16	CBIT(10)	16	CBIT(41)	16	CBIT(42)
17	CBIT(7)	17	CBIT(8)	17	CBIT(39)	17	CBIT(40)

Table 2.25: SCM Connector J104 (Continued)

Row A Pin #	Signal	Row B Pin #	Signal	Row C Pin #	Signal	Row D Pin #	Signal
18	CBIT(5)	18	CBIT(6)	18	CBIT(37)	18	CBIT(38)
19	CBIT(3)	19	CBIT(4)	19	CBIT(35)	19	CBIT(36)
20	CBIT(1)	20	CBIT(2)	20	CBIT(33)	20	CBIT(34)
21	GND	21	GND	21	GND	21	GND
22	GND	22	GND	22	GND	22	GND
23	DPS_LF [11-12]	23	DPS_LS[12]	23	DPS_HS[12]	23	DPS_HF[12]
24	DPS_LF [11-12]	24	DPS_LS[11]	24	DPS_HS[11]	24	DPS_HF[11]
25	PS_RPL_ - [9-10]	25	DPS_RPL_ -[11-12]	25	DPS_RPL_ +[9-10]	25	DPS_RPL_ +[11-12]
26	DPS_LF[9-10]	26	DPS_LS[10]	26	DPS_HS[10]	26	DPS_HF[10]
27	DPS_LF[9-10]	27	DPS_LS[9]	27	DPS_HS[9]	27	DPS_HF[9]
28	DPS_LF[7-8]	28	DPS_LS[8]	28	DPS_HS[8]	28	DPS_HF[8]
29	DPS_LF[7-8]	29	DPS_LS[7]	29	DPS_HS[7]	29	DPS_HF[7]
30	DPS_RPL_ -[5-6]	30	DPS_RPL_-[7-8]	30	DPS_RPL_ +[5-6]	30	DPS_RPL_ +[7-8]
31	DPS_LF[5-6]	31	DPS_LS[6]	31	DPS_HS[6]	31	DPS_HF[6]
32	DPS_LF[5-6]	32	DPS_LS[5]	32	DPS_HS[5]	32	DPS_HF[5]
33	DPS_LF[3-4]	33	DPS_LS[4]	33	DPS_HS[4]	33	DPS_HF[4]
34	DPS_LF[3-4]	34	DPS_LS[3]	34	DPS_HS[3]	34	DPS_HF[3]
35	DPS_RPL_ –[1-2]	35	DPS_RPL_ -[3-4]	35	DPS_RPL_ +[1-2]	35	DPS_RPL_ +[3-4]
36	DPS_LF[1-2]	36	DPS_LS[2]	36	DPS_HS[2]	36	DPS_HF[2]
37	DPS_LF[1-2]	37	DPS_LS[1]	37	DPS_HS[1]	37	DPS_HF[1]
38	GND	38	GND	38	GND	38	GND
39	WM_DC_ GUARD(4)	39	WM_DC_ LO(4)	39	SPARE[49]	39	SPARE[50]
40	WM_DC_ HI(4)	40	WM_DC_ GUARD(3)	40	SPARE[47]	40	SPARE[48]
41	WM_DC_ LO(3)	41	WM_DC_ HI(3)	41	SPARE[45]	41	SPARE[46]

Table 2.25: SCM Connector J104 (Continued)

Row A Pin #	Signal	Row B Pin #	Signal	Row C Pin #	Signal	Row D Pin #	Signal
42	WM_DC_ GUARD(2)	42	WM_DC_ LO(2)	42	SPARE[43]	42	SPARE[44]
43	WM_DC_ HI(2)	43	WM_DC_ GUARD(1)	43	SPARE[41]	43	SPARE[42]
44	WM_DC_ LO(1)	44	WM_DC_ HI(1)	44	SPARE[39]	44	SPARE[40]
45	GND	45	GND	45	SPARE[37]	45	SPARE[38]
46	GND	46	GND	46	SPARE[35]	46	SPARE[36]
47	WS_LF(4)	47	WS_HF(4)	47	SPARE[33]	47	SPARE[34]
48	WS_LS(4)	48	WS_ GUARD(4)	48	SPARE[31]	48	SPARE[32]
49	WS_HS(4)	49	WS_HS(3)	49	SPARE[29]	49	SPARE[30]
50	WS_LF(3)	50	WS_HF(3)	50	SPARE[27]	50	SPARE[28]
51	WS_LS(3)	51	WS_ GUARD(3)	51	SPARE[25]	51	SPARE[26]
52	WS_LF(2)	52	WS_HF(2)	52	SPARE[23]	52	SPARE[24]
53	WS_LS(2)	53	WS_ GUARD(2)	53	SPARE[21]	53	SPARE[22]
54	WS_HS(2)	54	WS_HS(1)	54	SPARE[19]	54	SPARE[20]
55	WS_LF(1)	55	WS_HF(1)	55	SPARE[17]	55	SPARE[18]
56	WS_LS(1)	56	WS_ GUARD(1)	56	SPARE[15]	56	SPARE[16]
57	GND	57	GND	57	SPARE[13]	57	SPARE[14]
58	SPARE[5]	58	SPARE[6]	58	SPARE[11]	58	SPARE[12]
59	SPARE[3]	59	SPARE[4]	59	SPARE[9]	59	SPARE[10]
60	SPARE[1]	60	SPARE[2]	60	SPARE[7]	60	SPARE[8]

Board Connectors

To see the locations of the board connectors, refer to Figure 2.15 on page 2-55.

PECHF Connector Pinout, JA1 - JA16

For the signal input / output list of connectors JA1 - JA16, refer to Table 2.24 on page 2-57.

PECHF Auxiliary Connector Pinout, J201 - J204

Table 2.23 on page 2-56 only lists the connections of J202. However, J201 - J204 have the same layout for their respective connections. The I / O differences are as follows.

- At row A, pin 25, the signal for J201 is instead THRG.
- The numbers in the brackets represent the first pin number of the signal's respective connector.

Table 2.26: PECHF Auxiliary Pinout

Row A Pin #	Signal	Row B Pin #	Signal	Row C Pin #	Signal	Row D Pin #	Signal
1	DPMTX_L1 [32]	1	DPMTX_L1G [32]	1	DPMTX_L2 [32]	1	DPMTX_L2G [32]
2	GND	2	DPAUX [32]	2	DPMTX_L1G [544]	2	DPMTX_L1 [544]
3	DPMTX_L2 [544]	3	DPMTX_L2G [544]	3	DPAUX [544]	3	GND
4	DPMTX_L1 G [288]	4	DPMTX_L1 [288]	4	DPMTX_L2G [288]	4	DPMTX_L1 [288]
5	DPAUX [288]	5	GND	5	DPMTX_L1 [800]	5	DPMTX_L1G [800]
6	DPMTX_L2 G [800]	6	DPMTX_L2 [800]	6	GND	6	DPAUX [800]
7	DPMTX_L1 [48]	7	DPMTX_L1G [48]	7	DPMTX_L2 [48]	7	DPMTX_L2G [48]
8	GND	8	DPAUX [48]	8	DPMTX_L1G [560]	8	DPMTX_L1 [560]
9	DPMTX_L2 [560]	9	DPMTX_L2G [560]	9	DPAUX [560]	9	GND

Table 2.26: PECHF Auxiliary Pinout (Continued)

Row A Pin #	Signal	Row B Pin #	Signal	Row C Pin #	Signal	Row D Pin #	Signal
10	DPMTX_ L1G [304]	10	DPMTX_L1 [304]	10	DPMTX_L2G [304]	10	DPMTX_L2 [304]
11	DPAUX [304]	11	GND	11	DPMTX_L1 [816]	11	DPMTX_L1 [816]
12	DPMTX_ L2G[816]	12	DPMTX_L2 [816]	12	GND	12	DPAUX [816]
13	DPMTX_L1 [64]	13	DPMTX_ L1G [64]	13	DPMTX_L2 [64]	13	DPMTX_L2G [64]
14	GND	14	DPAUX [64]	14	DPMTX_L1G [576]	14	DPMTX_L1 [576]
15	DPMTX_ L2 [576]	15	DPMTX_L2G [576]	15	DPAUX [576]	15	GND
16	DPMTX_ L1G [320]	16	DPMTX_L1 [320]	16	DPMTX_L2G [320]	16	DPMTX_L2 [320]
17	DPAUX [320]	17	GND	17	DPMTX_L1 [832]	17	DPMTX_L1G [832]
18	DPMTX_L2 G [832]	18	DPMTX_L2 [832]	18	GND	18	DPAUX [832]
19	DPMTX_L1 [80]	19	DPMTX_L1G [80]	19	DPMTX_L2 [80]	19	DPMTX_L2G [80]
20	GND	20	DPAUX [80]	20	DPMTX_L1G [592]	20	DPMTX_L1 [592]
21	DPMTX_L2 [592]	21	DPMTX_L2G [592]	21	DPAUX [592]	21	GND
22	DPMTX_L1 G [336]	22	DPMTX_L1 [336]	22	DPMTX_L2G [336]	22	DPMTX_L2 [336]
23	DPAUX [336]	23	GND	23	DPMTX_L1 [848]	23	DPMTX_L1G [848]
24	DPMTX_ L2G [848]	24	DPMTX_L2 [848]	24	GND	24	DPAUX [848]
25	N.C.	25	N.C.	25	N.C.	25	N.C.

Test Head Buffer Connector Pinout, JH1 - JH4

Table 2.27 shows the list of signals for Test Head Buffer 0(THBUF0), an interface board for the Test Head Bus Driver (THBDHF). The I/O for THBUF1, THBUF2, and THBUF3 have the same interface for their respective pin numbers.

Table 2.27: THBDHF Connector JH1

Pin #	Signal	Pin #	Signal
1	SEQ0	2	RESET0
3	+5V_THBD	4	GND
5	READ0	6	WRITE0
7	GND	8	GND
9	ALLPIN0	10	STB0
11	GND	12	GND
13	ADDR0[13]	14	ADDR0[12]
15	ADDR0[11]	16	ADDR0[10]
17	ADDR0[9]	18	ADDR0[8]
19	ADDR0[7]	20	ADDR0[6]
21	ADDR0[5]	22	ADDR0[4]
23	ADDR0[3]	24	ADDR0[2]
25	ADDR0[1]	26	ADDR0[0]
27	GND	28	GND
29	DATA0[15]	30	DATA0[14]
31	DATA0[13]	32	DATA0[12]
33	DATA0[11]	34	DATA0[10]
35	DATA0[9]	36	DATA0[8]
37	DATA0[7]	38	DATA0[6]
39	DATA0[5]	40	DATA0[4]
41	DATA0[3]	42	DATA0[2]
43	DATA0[1]	44	DATA0[0]
45	GND	46	+5V_THBD
47	THINT0	48	TEMPINT0
49	BUSY0	50	GND

Analog Crate Connectors

The following list the signal pinout for the boards that are located in the analog crate of the Fusion HF test head.

CBIT Connector JH5 - JH6

Table 2.28 lists the I/O for JH5, CBITS(1-32). The I/O for JH6 is the same layout, except for CBITS(33-64).

Table 2.28: CBITS(1-32) Connector

Pin #	Signal	Pin #	Signal
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	GND	8	GND
9	CBIT(1)	10	CBIT(2)
11	CBIT(3)	12	CBIT(4)
13	CBIT(5)	14	CBIT(6)
15	CBIT(7)	16	CBIT(8)
17	CBIT(9)	18	CBIT(10)
19	CBIT(11)	20	CBIT(12)
21	CBIT(13)	22	CBIT(14)
23	CBIT(15)	24	CBIT(16)
25	CBIT(17)	26	CBIT(18)
27	CBIT(19)	28	CBIT(20)
29	CBIT(21)	30	CBIT(22)
31	CBIT(23)	32	CBIT(24)
33	CBIT(25)	34	CBIT(26)
35	CBIT(27)	36	CBIT(28)
37	CBIT(29)	38	CBIT(30)
39	CBIT(31)	40	CBIT(32)
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND

Table 2.28: CBITS(1-32) Connector (Continued)

Pin #	Signal	Pin #	Signal
47	GND	48	GND
49	GND	50	GND

Device Power Source Connector JH7 - JH12

Table 2.29 lists the I/O for Device Power Source 1-2(DPS[1-2]). The layout for DPS[3-4], DPS[5-6], DPS[7-8], DPS[9-10], and DPS[11-12]are the same for their respective signals.

- DPS[1-2] connector JH7
- DPS[3-4] connector JH8
- DPS[5-6] connector JH9
- DPS[7-8] connector JH10
- DPS[9-10] connector JH11
- DPS[11-12] connector JH12

Table 2.29: Device Power Source Connector

Pin #	Signal	Pin #	Signal
1	DPS_LS(1)	2	DPS_HS(1)
3	DPS_LF[1-2]	4	DPS_HF(1)
5	DPS_LF[1-2]	6	DPS_HF(1)
7	DPS_LF[1-2]	8	DPS_HF(2)
9	DPS_LF[1-2]	10	DPS_HF(2)
11	DPS_LF[1-2]	12	DPS_HS(2)
13	DPS_LS(2)	14	GND
15	DPS_RPL_+[1-2]	16	DPS_RPL_-[1-2]

Measure System Connector JH13

Table 2.30 lists the I/O for JH13, the connection to Measure System (MS).

Table 2.30: Measure System Connector JH13

Pin #	Signal Name	Pin #	Signal Name
1	GND	2	GND
3	WS_GUARD[1]	4	WS_LS[1]
5	WS_HF[1]	6	WS_LF[1]
7	WS_HS[1]	8	WS_HS[2]
9	WS_GUARD[2]	10	WS_LS[2]
11	WS_HF[2]	12	WS_LF[2]
13	WS_GUARD[3]	14	WS_LS[3]
15	WS_HF[3]	16	WS_LF[3]
17	WS_HS[3]	18	WS_HS[4]
19	WS_GUARD[4]	20	WS_LS[4]
21	WS_HF[4]	22	WS_LF[4]
23	NC	24	NC
25	GND	26	GND
27	WM_DC_HI[1]	28	WM_DC_LO[1]
29	WM_DC_GUARD[1]	30	WM_DC_HI[2]
31	WM_DC_LO[2]	32	WM_DC_GUARD[2]
33	WM_DC_HI[3]	34	WM_DC_LO[3]
35	WM_DC_GUARD[3]	36	WM_DC_HI[4]
37	WM_DC_LO[4]	38	WM_DC_GUARD[4]
39	NC	40	NC

Spare Connector JH14

JH14 is a spare connector that can be user-defined.

Table 2.31: Spare Connector JH14

Pin #	Signal Name	Pin #	Signal Name
1	SCM_INTLK[1]	2	SCM_INTLK[2]
3	Spare[3]	4	Spare[4]

Table 2.31: Spare Connector JH14 (Continued)

Pin #	Signal Name	Pin #	Signal Name
5	Spare[5]	6	Spare[6]
7	Spare[7]	8	Spare[8]
9	Spare[9]	10	Spare[10]
11	Spare[11]	12	Spare[12]
13	Spare[13]	14	Spare[14]
15	Spare[15]	16	Spare[16]
17	Spare[17]	18	Spare[18]
19	Spare[19]	20	Spare[20]
21	Spare[21]	22	Spare[22]
23	Spare[23]	24	Spare[24]
25	Spare[25]	26	Spare[26]
27	Spare[27]	28	Spare[28]
29	Spare[29]	30	Spare[30]
31	Spare[31]	32	Spare[32]
33	Spare[33]	34	Spare[34]
35	Spare[35]	36	Spare[36]
37	Spare[37]	38	Spare[38]
39	Spare[39]	40	Spare[40]
41	Spare[41]	42	Spare[42]
43	Spare[43]	44	Spare[44]
45	Spare[45]	46	Spare[46]
47	Spare[47]	48	Spare[48]
49	Spare[49]	50	Spare[50]

Remote Power and Leak Sense Connector JH15

Leak signals are connected to JH15, and to the fused sense signals; Table 2.32 lists the I/O pinout.

Table 2.32: Remote Power and Leak Sense Connector JH15

Pin #	Signal	Pin #	Signal
1	LEAK0	2	VC15S

Table 2.32: Remote Power and Leak Sense Connector JH15 (Continued)

Pin #	Signal	Pin #	Signal
3	LEAK1	4	VC10S
5	GND	6	VC20S
7	LPBK64	8	LPBK0
9	GND	10	VE10S
11	GND	12	VE5S
13	LEAK2	14	VE15S
15	LEAK3	16	VC5S

Board ID Connector JH16

The Board ID connector, JH16, is connected to the HF Analog Backplane (HFABP). Table 2.33 shows the signal pinout.

Table 2.33: Board ID Connector JH16

Pin #	Signal	Pin #	Signal
1	+5V_THBD	2	GND
3	+5V_THBD	4	GND
5	+5V_THBD	6	H_RET
7	+5V_THBD	8	EE_DATA
9	GND	10	EE_EN
11	GND	12	EE_CLK
13	-5V_THBD	14	+5_EEPROM
15	-5V_THBD	16	GND
17	-5V_THBD	18	GND
19	-5V_THBD	20	+10V_THBD

High Speed Clock Connector, JG1 - JG64

Table 2.34 lists the signal pinout for the High Speed Clock (HSCK) connectors, JG1 - JG64.

Table 2.34: HSCK Connector

Pin #	Signal
1	GND
2	HSCKA[n]
3	HSCKB[n]

HF Analog Backplane (HFABP)

The HF Analog Backplane (HFABP) supports 35 Head Card slots for analog test head boards and the Digital THBDHF board. Power, EEPROM, and Test Head Bus signals are provided to the 8 modules located on the sides of the head. The EEPROM signals are connected to the Digital Backplane

Analog Crate Layout

The signals from the boards in the analog crate and the mainframe cables are routed to three 240 high density interface (HDI) connectors and sixteen RF connectors of the Digital System Configuration Module (DSCM, also known as family board).

Figure 2.9 on page 2-17 shows the layout of the HF analog backplane.

Figure 2.16 through Figure 2.23 show the layouts of the connections of the boards in the HF test head analog crate.

- Figure 2.16, Octal AP Board, on page 2-70
- Figure 2.17, SMS/HF User Board, on page 2-71
- Figure 2.18, RF01/02, RF User Board, on page 2-72
- Figure 2.19, WBS/RF User Board, on page 2-73
- Figure 2.20, TMU Buffer Board, on page 2-74
- Figure 2.21, MS Buffer Board, on page 2-75

- Figure 2.22, THBIF Board, on page 2-76
- Figure 2.23, THBDHF Board, on page 2-77

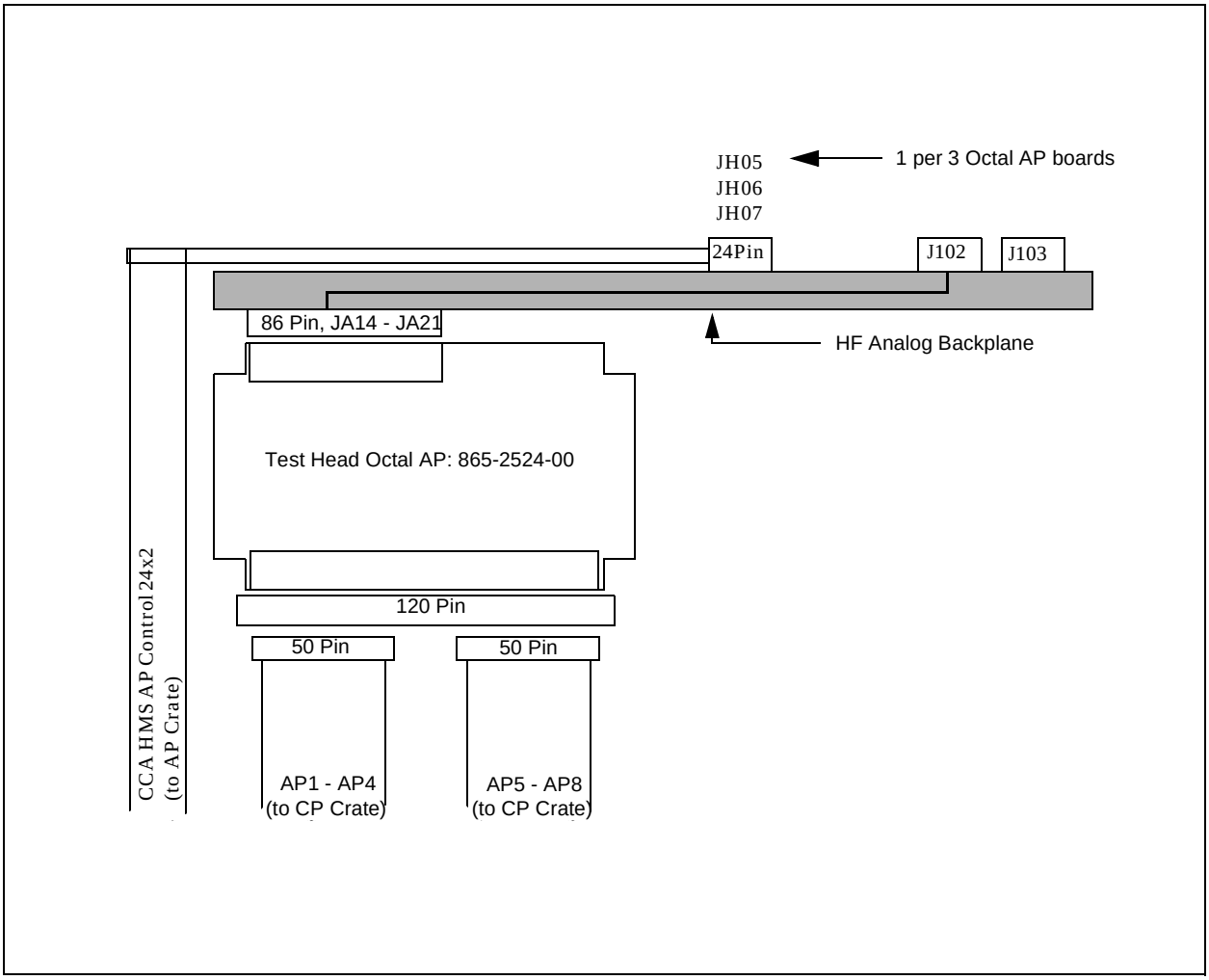

Figure 2.16: Octal AP Board

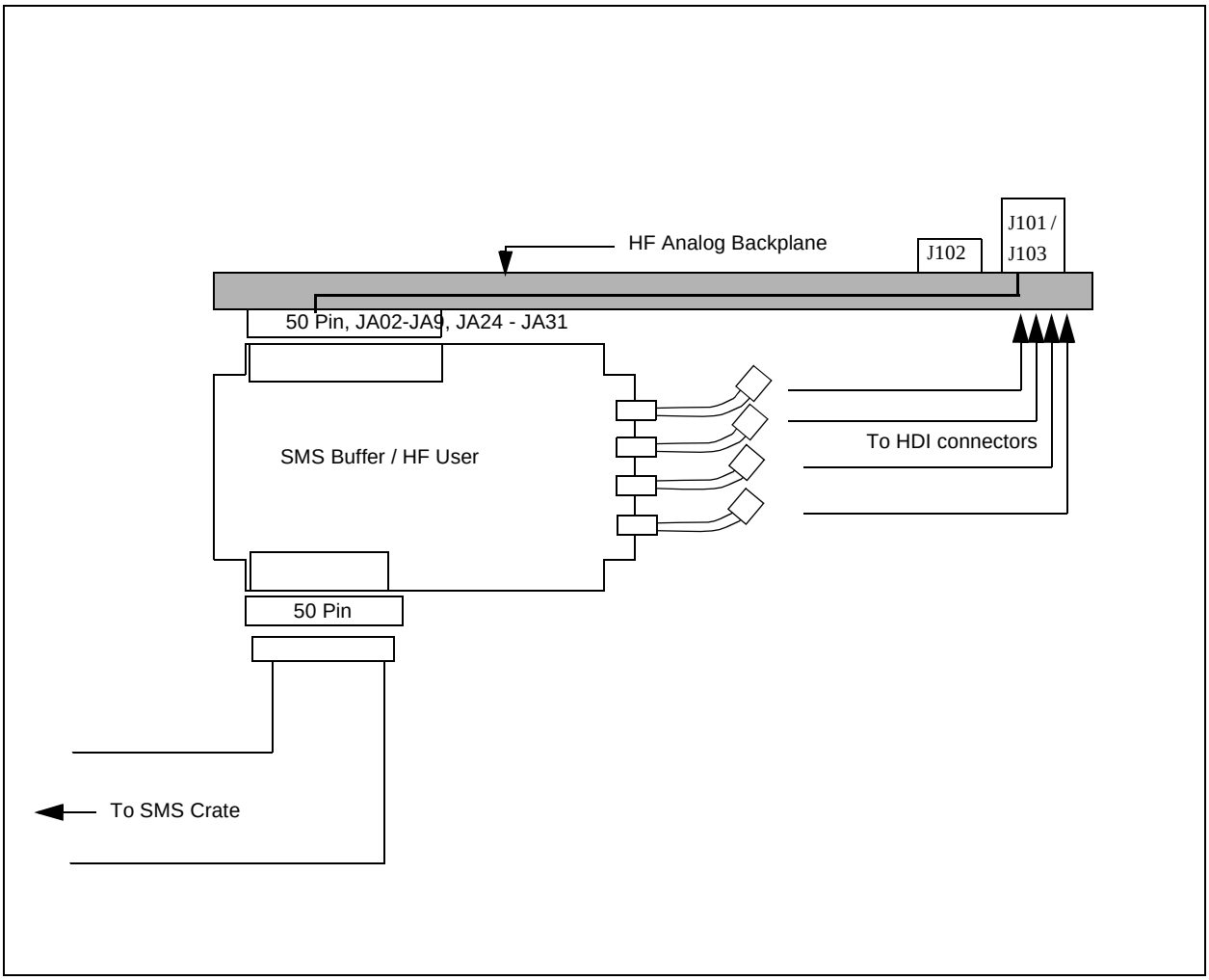

Figure 2.17: SMS/HF User Board

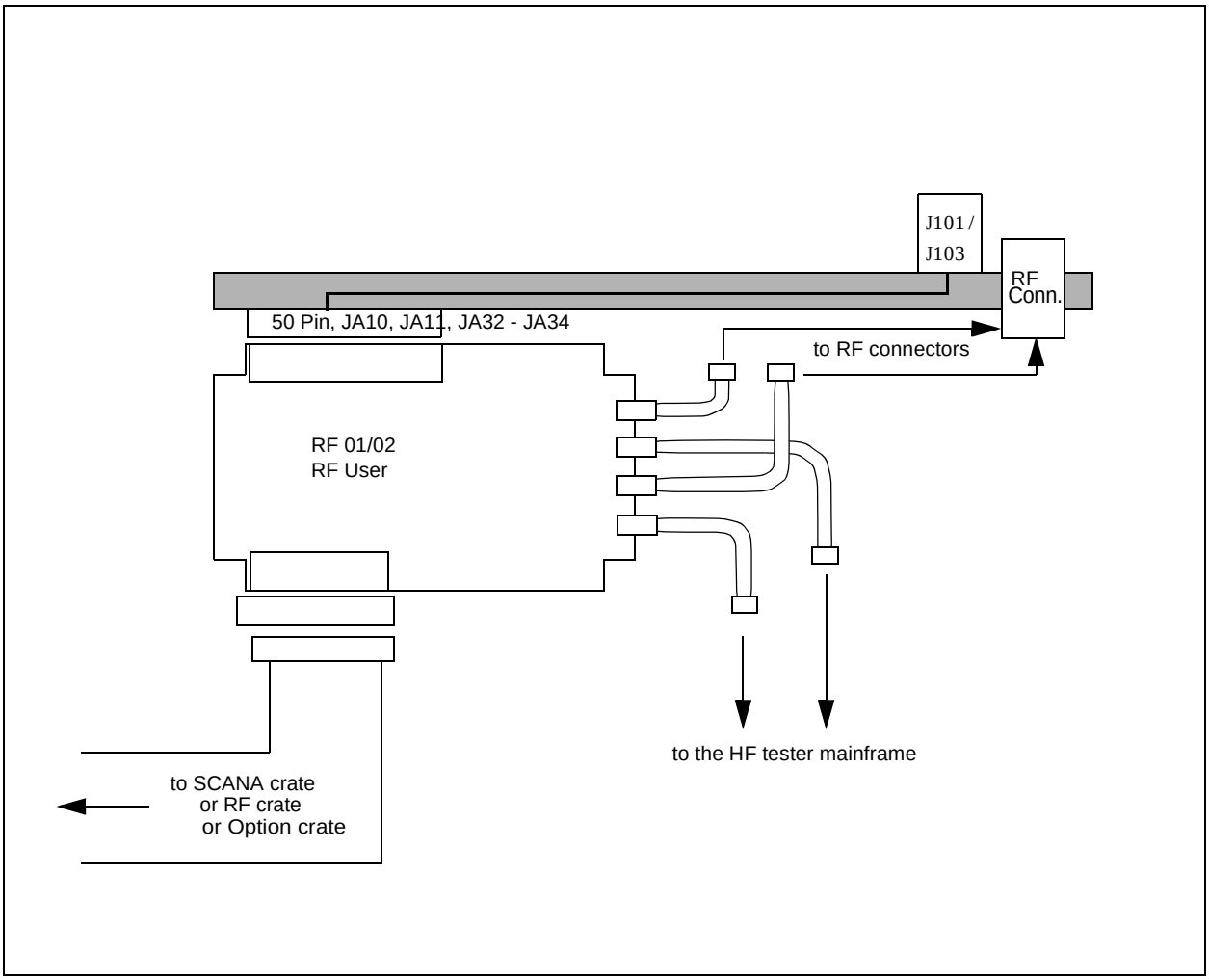

Figure 2.18: RF01/02, RF User Board

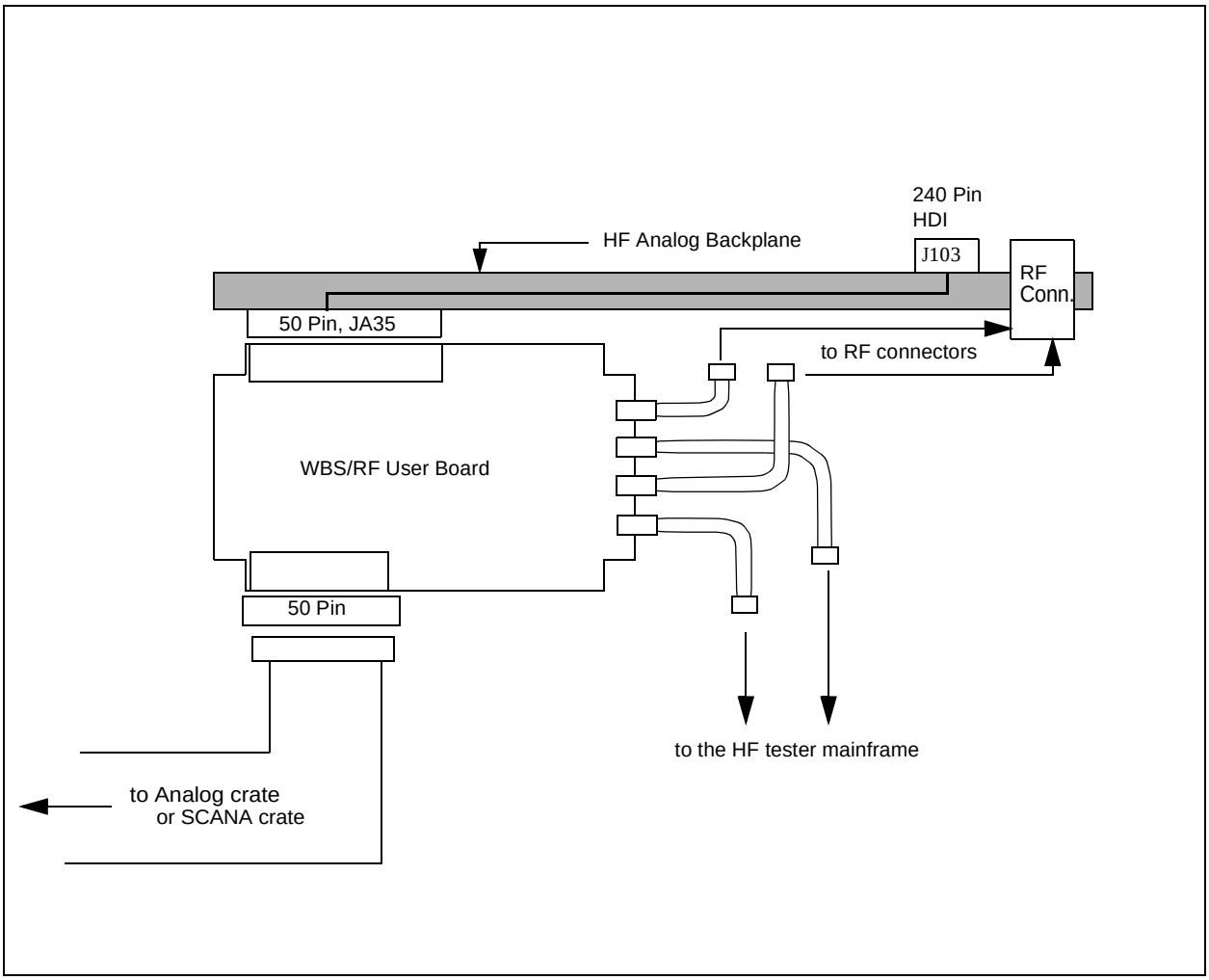

Figure 2.19: WBS/RF User Board

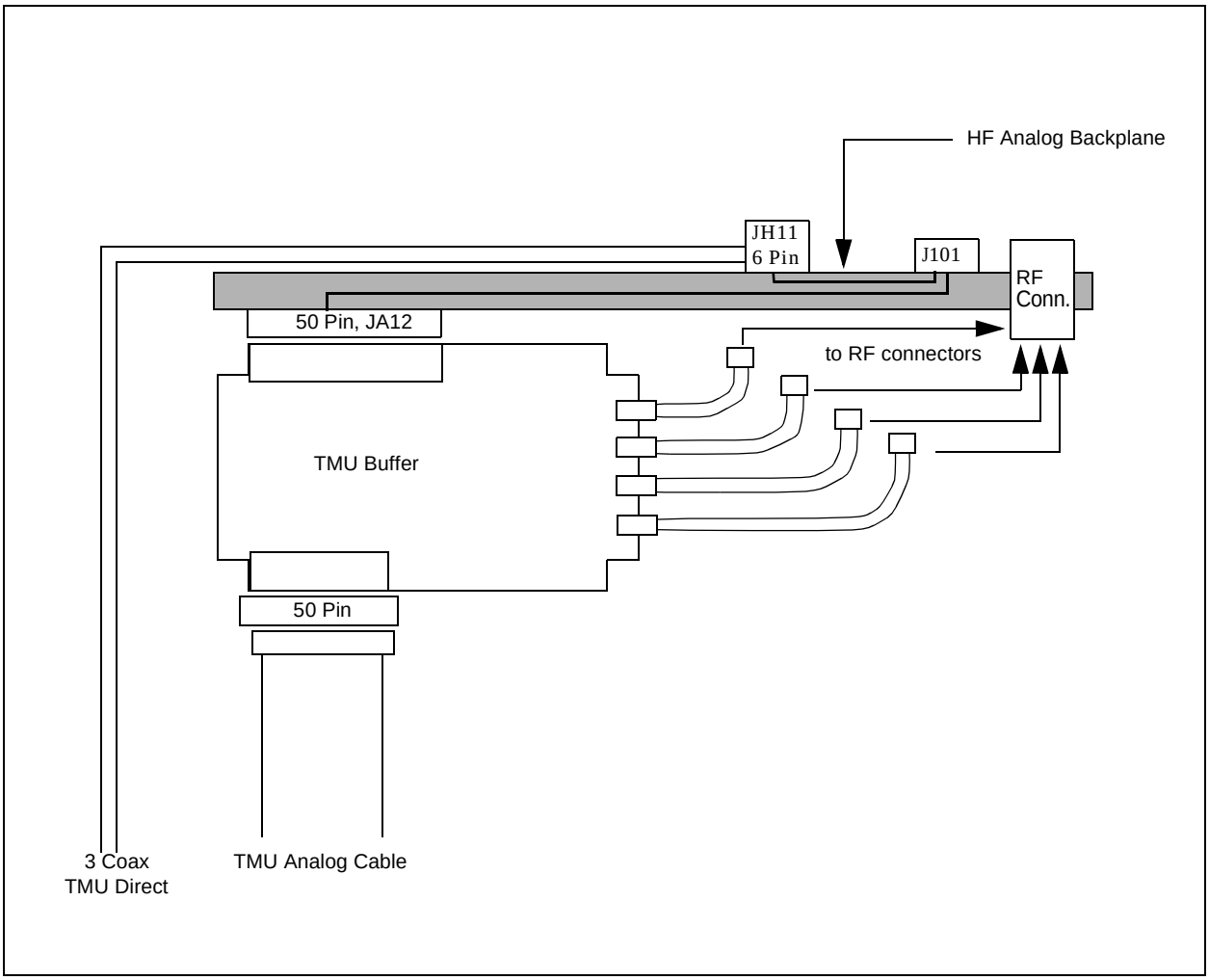

Figure 2.20: TMU Buffer Board

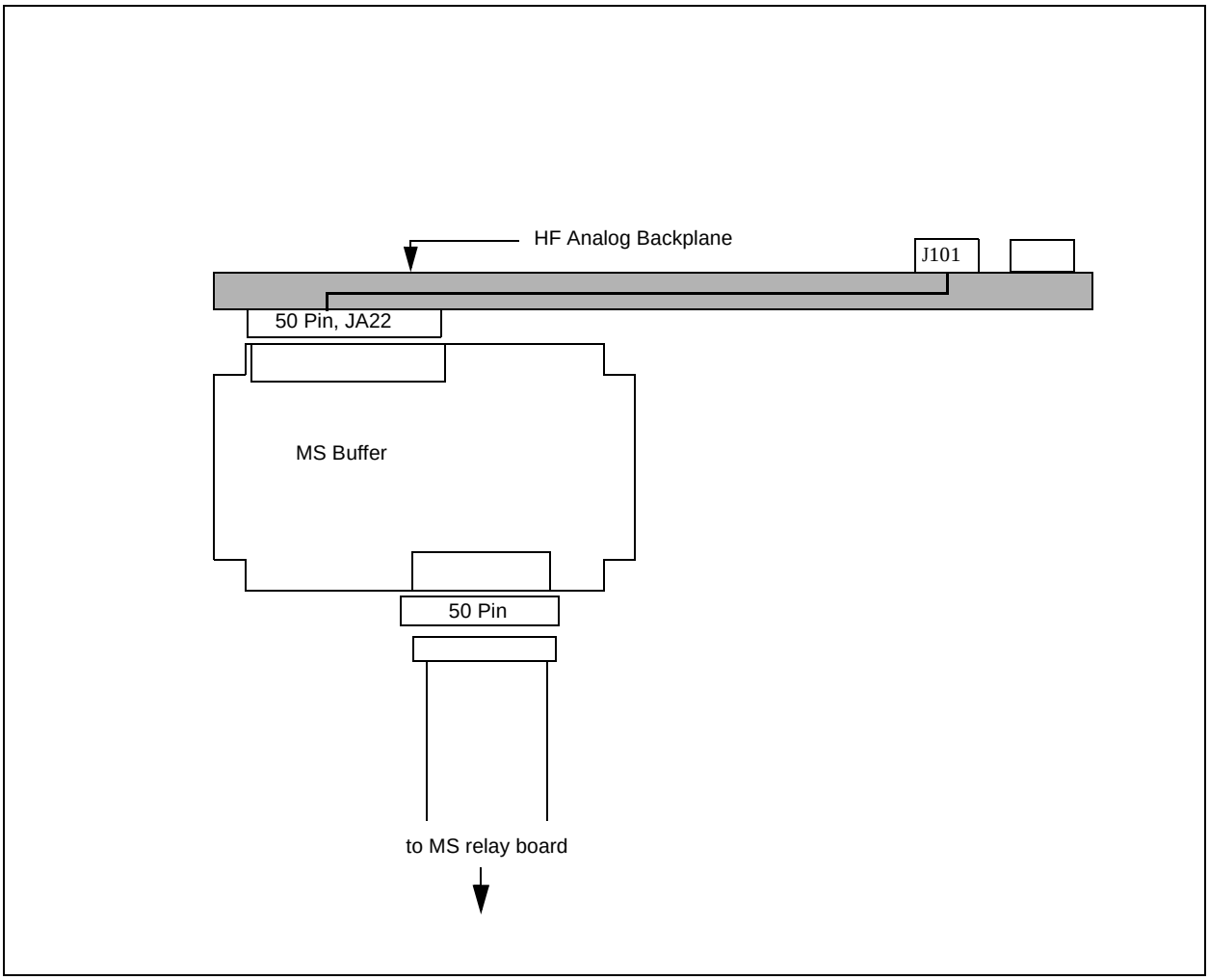

Figure 2.21: MS Buffer Board

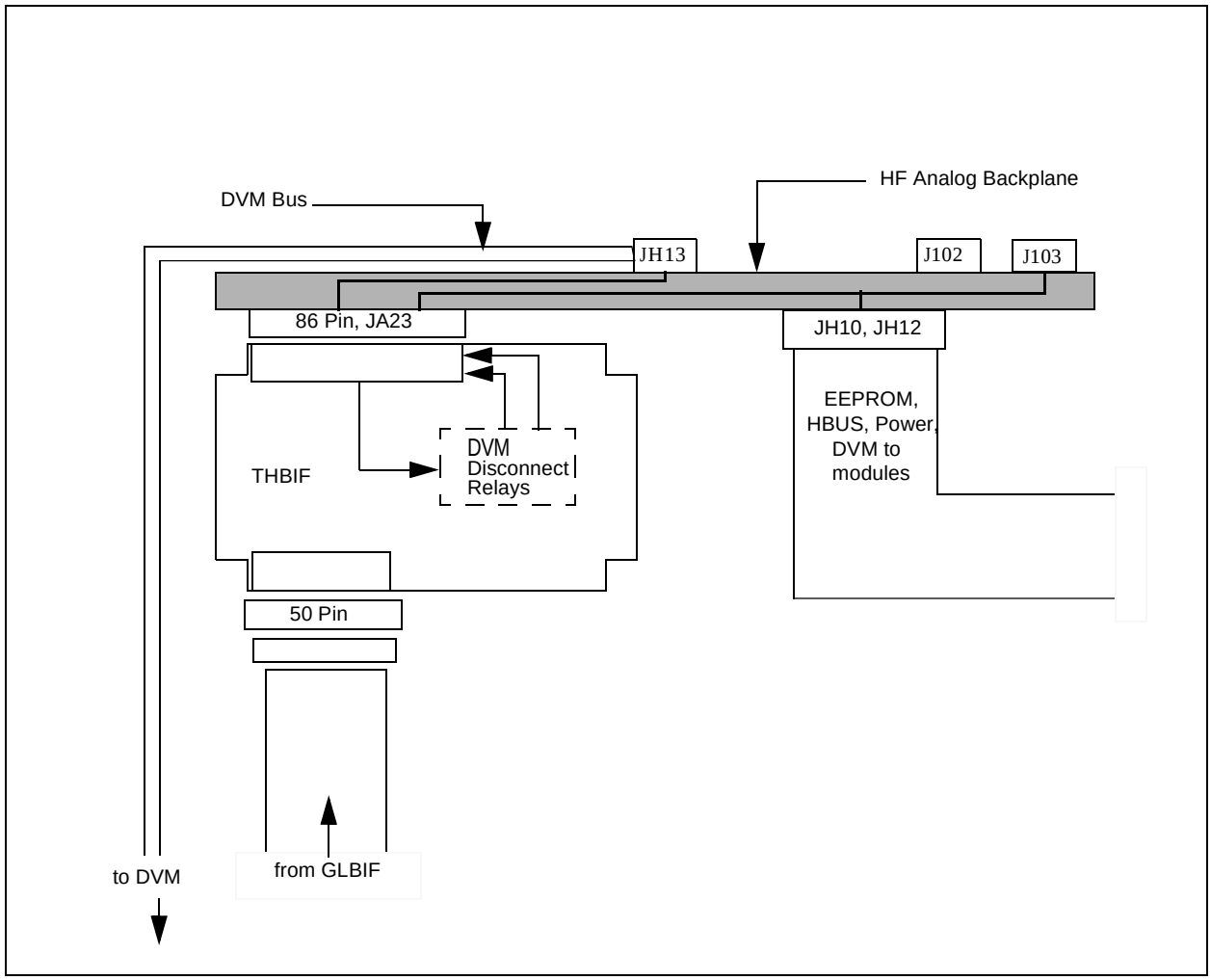

Figure 2.22: THBIF Board

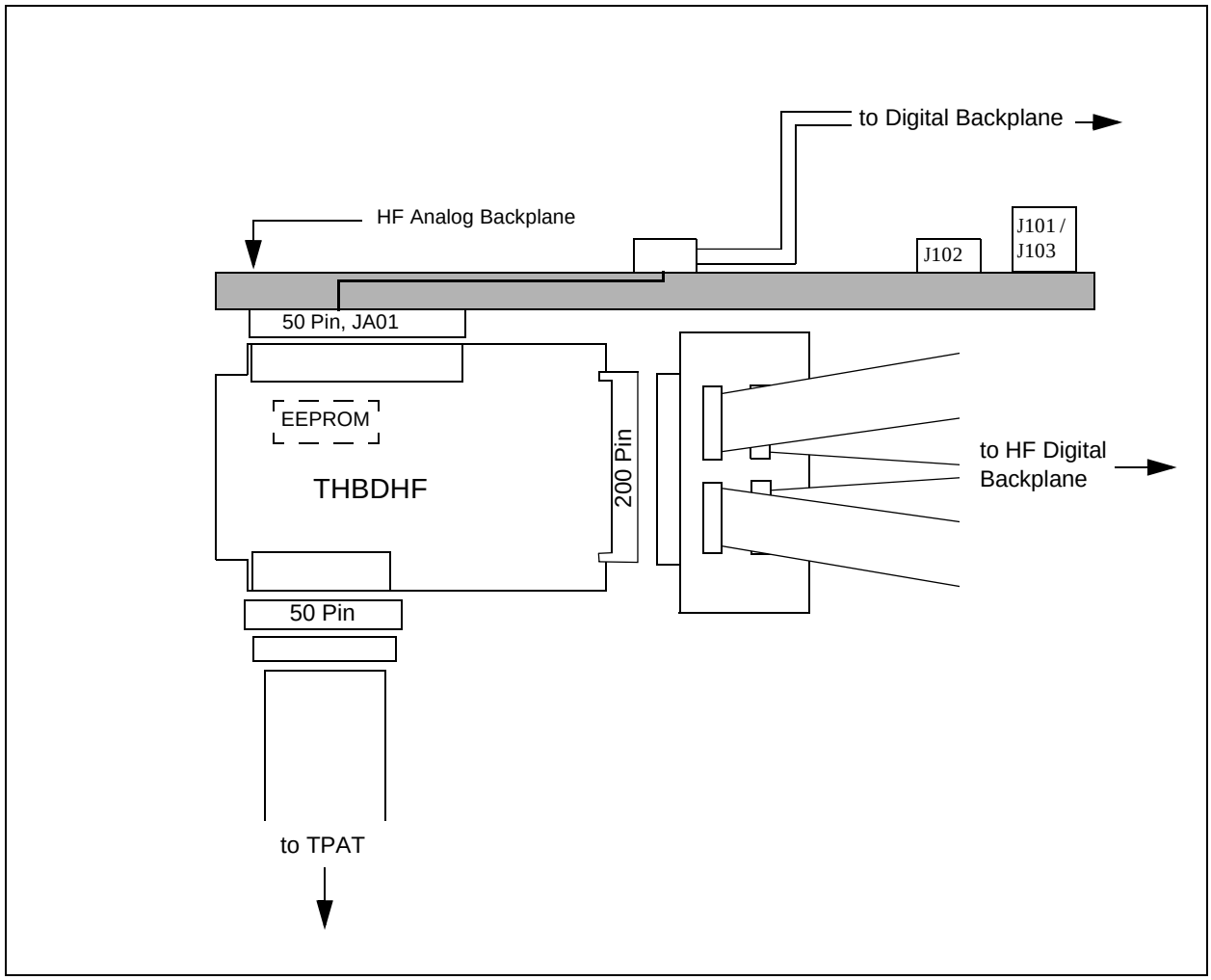

Figure 2.23: THBDHF Board

High Density Interface (HDI) ConnectorPinout

Following are the lists of I/O pinout for the HDI connectors, J101 - J103.

J101, HDI Connector

Table 2.35 shows the pinout of the HD I connector J101.

Table 2.35: HDI Pinout J101

Pin No.	Row D	Row C	Row B	Row A
1	UTH_JA02_IC1	UTH_JA02_IC2	UTH_JA02_IC3	TUM_DIR_CHAN[1]
2	UTH_JA02_IC4	UTH_JA02_IC5	UTH_JA02_IC6	H_RET
3	UTH_JA02_IC7	UTH_JA02_IC8	UTH_JA02_IC9	TUM_DIR_CHAN[2]
4	UTH_JA02_1C10	UTH_JA02_IC11	UTH_JA02_IC12	H_RET
5	UTH_JA02_IC13	UTH_JA02_IC14	UTH_JA02_IC15	TUM_DIR_CHAN[3]
6	UTH_JA02_IC16	UTH_JA02_IC17	UTH_JA02_IC18	H_RET
7	UTH_JA02_IC19	UTH_JA02_ic20	UTH_JA02_ic21	UTH_JA02_ic22
8	UTH_JA02_ic23	UTH_JA02_ic24	UTH_JA03_IC1	UTH_JA02_IC2
9	UTH_JA03_IC3	UTH_JA03_IC4	H_RET	SMS_S+[1]
10	UTH_JA03_IC5	UTH_JA03_IC6	H_RET	SMS_S-[1]
11	UTH_JA03_IC7	UTH_JA03_IC8	UTH_JA03_IC9	UTH_JA03_IC10
12	UTH_JA03_IC11	UTH_JA03_IC12	H_RET	SMS_M+[1]
13	UTH_JA03_IC13	UTH_JA03_IC14	H_RET	SMS_M-[1]
14	UTH_JA03_IC15	UTH_JA03_IC16	UTH_JA03_IC17	UTH_JA03_IC18
15	UTH_JA03_IC19	UTH_JA03_IC20	H_RET	SMS_S+[2]
16	UTH_JA03_IC21	UTH_JA03_IC22	H_RET	SMS_S-[2]
17	UTH_JA03_IC23	UTH_JA03_IC24	UTH_JA06_IC1	UTH_JA06_IC2
18	UTH_JA06_IC3	UTH_JA06_IC4	H_RET	SMS_M+[2]
19	UTH_JA06_IC5	UTH_JA06_IC6	H_RET	SMS_M-[2]
20	UTH_JA06_IC7	UTH_JA06_IC8	UTH_JA06_IC9	UTH_JA06_IC10
21	H_RET	UTH_JA06_IC11	H_RET	SMS_S+[3]
22	TMU_BUF+CHAN[1]	UTH_JA06_IC12	H_RET	SMS_S-[3]
23	H_RET	UTH_JA07_IC1	UTH_JA07_IC2	UTH_JA07_IC3

Table 2.35: HDI Pinout J101 (Continued)

Pin No.	Row D	Row C	Row B	Row A
24	TMU_BUF+CHAN[3]	UTH_JA07_IC4	H_RET	SMS_M+[3]
25	H_RET	UTH_JA07_IC5	H_RET	SMS_M-[3]
26	TMU_BUF+CHAN[3]	UTH_JA07_IC6	UTH_JA07_IC7	UTH_JA07_IC8
27	H_RET	UTH_JA07_IC9	H_RET	SMS_S+[4]
28	UTH_JA07_IC10	UTH_JA07_IC11	H_RET	SMS_S-[4]
29	UTH_JA07_IC12	UTH_JA08_IC1	UTH_JA08_IC2	UTH_JA08_IC3
30	UTH_JA08_IC4	UTH_JA08_IC5	H_RET	SMS_M+[4]
31	UTH_JA08_IC6	UTH_JA08_IC7	H_RET	SMS_M-[4]
32	UTH_JA08_IC8	UTH_JA08_IC9	UTH_JA08_IC10	UTH_JA08_IC11
33	UTH_JA08_IC12	UTH_JA09_IC1	H_RET	SMS_S+[9]
34	UTH_JA09_IC2	UTH_JA09_IC3	H_RET	SMS_S-[9]
35	UTH_JA09_IC4	UTH_JA09_IC5	UTH_JA09_IC6	UTH_JA09_IC7
36	UTH_JA09_IC8	UTH_JA09_IC9	H_RET	SMS_M+[9]
37	UTH_JA09_IC10	UTH_JA09_IC11	H_RET	SMS_M-[9]
38	UTH_JA09_IC12	UTH_JA10_IC1	UTH_JA10_IC2	UTH_JA10_IC3
39	UTH_JA10_IC4	UTH_JA10_IC5	H_RET	SMS_S+[10]
40	UTH_JA10_IC6	UTH_JA10_IC7	H_RET	SMS_S-[10]
41	UTH_JA10_IC8	UTH_JA10_IC9	UTH_JA10_IC10	UTH_JA10_IC11
42	UTH_JA10_IC12	UTH_JA11_IC1	H_RET	SMS_M+[10]
43	UTH_JA11_IC2	UTH_JA11_IC3	H_RET	SMS_M-[10]
44	UTH_JA11_IC4	UTH_JA11_IC5	UTH_JA11_IC6	UTH_JA11_IC7
45	UTH_JA11_IC8	UTH_JA11_IC9	H_RET	SMS_S+[11]
46	UTH_JA11_IC10	UTH_JA11_IC11	H_RET	SMS_S-[11]
47	UTH_JA11_IC12	UTH_JA12_IC1	UTH_JA12_IC2	UTH_JA12_IC3
48	UTH_JA12_IC4	UTH_JA12_IC5	H_RET	SMS_M+[11]
49	UTH_JA12_IC6	UTH_JA12_IC7	H_RET	SMS_M-[11]
50	UTH_JA12_IC8	UTH_JA12_IC9	UTH_JA12_IC10	UTH_JA12_IC11
51	UTH_JA12_IC12	UTH_JA13_IC1	H_RET	SMS_S+[12]
52	UTH_JA13_IC1	UTH_JA13_IC2	H_RET	SMS_S-[12]

Table 2.35: HDI Pinout J101 (Continued)

Pin No.	Row D	Row C	Row B	Row A
53	UTH_JA13_IC3	UTH_JA13_IC5	UTH_JA13_IC6	UTH_JA13_IC7
54	UTH_JA13_IC8	UTH_JA13_IC9	H_RET	SMS_M+[12]
55	UTH_JA13_IC10	UTH_JA13_IC11	H_RET	SMS_M-[12]
56	UTH_JA13_IC12	NC	NC	NC
57	NC	NC	NC	NC
58	NC	NC	+40V_SA	+15V_SA
59	+5V_SA	+5V_SA	-40V_SA	-15V_SA
60	-5V_SA	-5V_SA	+12_SA	-12_SA

J102, HDI Connector

Table 2.36 lists the pinout of the HDI connector J102.

Table 2.36: HDI Pinout J102

Pin No.	Row D	Row C	Row B	Row A
1	AP_G_S[49]	AP[49]	AP_G_S[1]	AP[1]
2	AP_G_S[50]	AP[50]	AP_G_S[2]	AP[2]
3	AP_G_S[51]	AP[51]	AP_G_S[3]	AP[3]
4	AP_G_S[52]	AP[52]	AP_G_S[4]	AP[4]
5	AP_G_S[53]	AP[53]	AP_G_S[5]	AP[5]
6	AP_G_S[54]	AP[54]	AP_G_S[6]	AP[6]
7	AP_G_S[55]	AP[55]	AP_G_S[7]	AP[7]
8	AP_G_S[56]	AP[56]	AP_G_S[8]	AP[8]
9	AP_G_S[57]	AP[57]	AP_G_S[9]	AP[9]
10	AP_G_S[58]	AP[58]	AP_G_S[10]	AP[10]
11	AP_G_S[59]	AP[59]	AP_G_S[11]	AP[11]
12	AP_G_S[60]	AP[60]	AP_G_S[12]	AP[12]
13	AP_G_S[61]	AP[61]	AP_G_S[13]	AP[13]
14	AP_G_S[62]	AP[62]	AP_G_S[14]	AP[14]
15	AP_G_S[63]	AP[63]	AP_G_S[15]	AP[15]

Table 2.36: HDI Pinout J102 (Continued)

Pin No.	Row D	Row C	Row B	Row A
16	AP_G_S[64]	AP[64]	AP_G_S[16]	AP[16]
17	APMTX_L1F[49-64]	APMTX_L1S[49-64]	AP_G_S[17]	AP[17]
18	APMTX_L2F[49-64]	APMTX_L2S[49-64]	AP_G_S[18]	AP[18]
19	NC	NC	AP_G_S[19]	AP[19]
20	WM_AC_HI[1]	WM_AC_LO[1]	AP_G_S[20]	AP[20]
21	WM_AC_HI[23]	WM_AC_LO[2]	AP_G_S[21]	AP[21]
22	WM_AC_HI[3]	WM_AC_LO[3]	AP_G_S[22]	AP[22]
23	WM_AC_HI[4]	WM_AC_LO[4]	AP_G_S[23]	AP[23]
24	NC	NC	AP_G_S[24]	AP[24]
25	NC	H_CLK[5]	APMTX_L1F[1-24]	APMTX_L1S[1-24]
26	+5V_EEPROM	H_CLK[6]	APMTX_L2F[1-24]	APMTX_L2S[1-24]
27	EE_CLK[0]	H_CLK[7]	AP_G_2[25]	AP[25]
28	EE_CLK[1]	H_EN[4]	AP_G_2[26]	AP[26]
29	EE_EN[0]	H_EN[5]	AP_G_2[27]	AP[27]
30	EE_EN[1]	H_EN[6]	AP_G_2[28]	AP[28]
31	EE_DATA[0]	H_DATA	AP_G_2[29]	AP[299]
32	EE_DATA[1]	H_REG_STB	AP_G_2[30]	AP[30]
33	SA_DZ	H_RESET	AP_G_2[31]	AP[31]
34	H_RET	H_RET	AP_G_2[32]	AP[32]
35	PM1_TO_DUT	PM1_TO_DUT*	AP_G_2[33]	AP[33]
36	H_RET	H_RET	AP_G_2[34]	AP[34]
37	PM1_FROM_DUT	PM1_FROM_DUT*	AP_G_2[35]	AP[35]
38	H_RET	H_RET	AP_G_2[36]	AP[36]
39	NC	NC	AP_G_2[37]	AP[37]
40	NC	NC	AP_G_2[38]	AP[38]
41	NC	NC	AP_G_2[39]	AP[39]
42	NC	NC	AP_G_2[40]	AP[40]
43	NC	NC	AP_G_2[41]	AP[41]
44	NC	NC	AP_G_2[42]	AP[42]

Table 2.36: HDI Pinout J102 (Continued)

Pin No.	Row D	Row C	Row B	Row A
45	NC	NC	AP_G_2[43]	AP[43]
46	UTH_JA24_IC1	UTH_JA24_IC2	AP_G_2[44]	AP[44]
47	UTH_JA24_IC3	UTH_JA24_IC4	AP_G_2[45]	AP[45]
48	UTH_JA24_IC5	UTH_JA24_IC6	AP_G_2[46]	AP[46]
49	UTH_JA24_IC7	UTH_JA24_IC8	AP_G_2[47]	AP[47]
50	UTH_JA24_IC9	UTH_JA24_IC10	AP_G_2[48]	AP[48]
51	UTH_JA24_IC11	UTH_JA24_IC12	APMTX_L1F[25-48]	APMTX_L1FS[25-48]
52	UTH_JA25_IC1	UTH_JA25_IC2	APMTX_L2F[25-48]	APMTX_L2S[25-48]
53	UTH_JA25_IC3	UTH_JA25_IC4	H_RET	H_RET
54	UTH_JA25_IC5	UTH_JA25_IC6	H_RET	WM_256V_H1
55	UTH_JA25_IC7	UTH_JA25_IC8	H_RET	H_RET
56	UTH_JA25_IC9	UTH_JA25_IC10	NC	NC
57	UTH_JA25_IC11	UTH_JA25_IC12	NC	NC
58	H_RET	H_RET	+40V_SA	+15V_SA
59	+5V_SA	+5V_SA	-40V_SA	-15V_SA
60	-5V_SA	-5V_SA	+12_SA	-12_SA

J103, HDI Connector

Table 2.37 lists the pinout of the HDI connector J103.

Table 2.37: HDI Pinout J103

Pin No.	Row D	Row C	Row B	Row A
1	F_DVM_FORCE_LO	F_DVM_SENSE_LO	F_DVM_SENSE_HI	F_DVM_FORCE_HI
2	F_DVM_GUARD_LO	H_REG	H_RET	H_RET
3	UTH_JA26_IC1	UTH_JA26_IC2	UTH_JA26_IC3	UTH_JA26_IC7
4	UTH_JA26_IC5	UTH_JA26_IC6	H_RET	SMS_S+[5]
5	UTH_JA26_IC7	UTH_JA26_IC8	H_RET	SMS_S-[5]
6	UTH_JA26_IC9	UTH_JA26_IC10	UTH_JA26_IC11	UTH_JA26_IC12
7	UTH_JA27_IC1	UTH_JA27_IC2	H_RET	SMS_M+[5]

Table 2.37: HDI Pinout J103 (Continued)

Pin No.	Row D	Row C	Row B	Row A
8	UTH_JA27_IC3	UTH_JA27_IC4	H_RET	SMS_M-[5]
9	UTH_JA27_IC5	UTH_JA27_IC6	UTH_JA27_IC7	UTH_JA27_IC8
10	UTH_JA27_IC9	UTH_JA27_IC10	H_RET	SMS_S+[6]
11	UTH_JA27_IC11	UTH_JA27_IC12	H_RET	SMS_S-[6]
12	UTH_JA28_IC1	UTH_JA28_IC2	UTH_JA28_IC3	UTH_JA28_IC4
13	UTH_JA28_IC5	UTH_JA28_IC6	H_RET	SMS_M+[6]
14	UTH_JA28_IC7	UTH_JA28_IC8	H_RET	SMS_M-[6]
15	UTH_JA28_IC9	UTH_JA28_IC10	UTH_JA28_IC11	UTH_JA28_IC12
16	UTH_JA29_IC1	UTH_JA29_IC2	H_RET	SMS_S+[7]
17	UTH_JA29_IC3	UTH_JA29_IC4	H_RET	SMS_S-[7]
18	UTH_JA29_IC5	UTH_JA29_IC6	UTH_JA29_IC7	UTH_JA29_IC8
19	UTH_JA29_IC9	UTH_JA29_IC10	H_RET	SMS_M+[7]
20	UTH_JA29_IC11	UTH_JA29_IC12	H_RET	SMS_M-[7]
21	UTH_JA30_IC1	UTH_JA30_IC2	UTH_JA30_IC3	UTH_JA30_IC4
22	UTH_JA30_IC5	UTH_JA30_IC6	H_RET	SMS_S+[8]
23	UTH_JA30_IC7	UTH_JA30_IC8	H_RET	SMS_S-[8]
24	UTH_JA30_IC9	UTH_JA30_IC10	UTH_JA30_IC11	UTH_JA30_IC12
25	UTH_JA31_IC1	UTH_JA31_IC2	H_RET	SMS_M+[8]
26	UTH_JA31_IC3	UTH_JA31_IC4	H_RET	SMS_M-[8]
27	UTH_JA31_IC5	UTH_JA31_IC6	UTH_JA31_IC7	UTH_JA31_IC8
28	UTH_JA31_IC9	UTH_JA31_IC10	H_RET	SMS_S+[13]
29	UTH_JA31_IC11	UTH_JA31_IC12	H_RET	SMS_S-[13]
30	UTH_JA32_IC1	UTH_JA32_IC2	UTH_JA32_IC3	UTH_JA32_IC4
31	UTH_JA32_IC5	UTH_JA32_IC6	H_RET	SMS_M+[13]
32	UTH_JA32_IC7	UTH_JA32_IC8	H_RET	SMS_M-[13]
33	UTH_JA32_IC9	UTH_JA32_IC10	UTH_JA32_IC11	UTH_JA32_IC12
34	UTH_JA32_IC13	UTH_JA32_IC14	H_RET	SMS_S+[14]
35	UTH_JA32_IC15	UTH_JA32_IC16	H_RET	SMS_S-[14]
36	UTH_JA32_IC17	UTH_JA32_IC18	UTH_JA32_IC19	UTH_JA32_IC20

Table 2.37: HDI Pinout J103 (Continued)

Pin No.	Row D	Row C	Row B	Row A
37	UTH_JA32_IC21	UTH_JA32_IC22	H_RET	SMS_M+[14]
38	UTH_JA32_IC23	UTH_JA32_IC24F	H_RET	SMS_M-[14]
39	UTH_JA33_IC1	UTH_JA33_IC2	UTH_JA33_IC3	UTH_JA33_IC4
40	UTH_JA33_IC5	UTH_JA33_IC6	H_RET	SMS_S+[15]
41	UTH_JA33_IC7	UTH_JA33_IC8	H_RET	SMS_S-[15]
42	UTH_JA33_IC9	UTH_JA33_IC10	UTH_JA33_IC	UTH_JA33_IC
43	UTH_JA33_IC11	UTH_JA33_IC12	H_RET	SMS_M+[15]
44	UTH_JA33_IC13	UTH_JA33_IC14	H_RET	SMS_M-[15]
45	UTH_JA33_IC15	UTH_JA33_IC16	UTH_JA33_IC17	UTH_JA33_IC18
46	UTH_JA33_IC19	UTH_JA33_IC20	H_RET	SMS_S+[16]
47	UTH_JA33_IC21	UTH_JA33_IC22	H_RET	SMS_S-[16]
48	UTH_JA34_IC1	UTH_JA34_IC2	UTH_JA34_IC3	UTH_JA34_IC4
49	UTH_JA34_IC5	UTH_JA34_IC6	H_RET	SMS_M+[16]
50	UTH_JA34_IC7	UTH_JA34_IC8	H_RET	SMS_M-[16]
51	UTH_JA34_IC9	UTH_JA34_IC10	UTH_JA34_IC11	UTH_JA34_IC12
52	UTH_JA34_IC13	UTH_JA34_IC14	UTH_JA34_IC15	UTH_JA34_IC16
53	UTH_JA34_IC17	UTH_JA34_IC18	UTH_JA34_IC19	UTH_JA34_IC20
54	UTH_JA34_IC21	UTH_JA34_IC22	UTH_JA34_IC23	UTH_JA34_IC24
55	UTH_JA35_IC1	UTH_JA35_IC2	UTH_JA35_IC3	UTH_JA35_IC4
56	UTH_JA35_IC5	UTH_JA35_IC6	UTH_JA35_IC7	UTH_JA35_IC8
57	UTH_JA35_IC9	UTH_JA35_IC10	UTH_JA35_IC11	UTH_JA35_IC12
58	UTH_JA35_IC13	UTH_JA35_IC14	UTH_JA35_IC15	UTH_JA35_IC16
59	UTH_JA35_IC17	UTH_JA35_IC18	UTH_JA35_IC19	UTH_JA35_IC20
60	UTH_JA35_IC21	UTH_JA35_IC22	UTH_JA35_IC23	UTH_JA35_IC24

OSSP Mapping: RF Connectors

Table 2.38 lists the mapping of the OSSP RF connectors.

Table 2.38: OSSP Mapping (RF Connectors)

Slot	Pin Card	OSSP Connector
JA02	RF USER	J301
		J302
JA03	RF USER	J303
		J304
JA04	CTMU BUFFER	J305
		J306
		J307
		J308
JA32	RF USER	J309
		J310
JA33	RF USER	J311
		J312
JA34	RF USER	J313
		J314
JA35	RF USER	J315
		J316

Compatible Test Head Printed Circuit Boards

The following printed circuit boards can be installed in either the Fusion HF analog crate or the Fusion HT analog crate. Detailed information for each board is available in the online manual.

- Octal AP: Octal Analog Pins
- APC: Analog Pin Control
- SMS: Sequenced Measure System
- CTMU: Central Time Measure Unit
- HF User: Prototype board for user-defined circuits

- THP: Test Head Prototype, for user-defined circuits
- WBS: Wide Band Sampler

Docking Test Head To Prober / Handler

Two methods of docking the test head to a prober (or handler) are possible: soft docking and hard docking. In either case, special tools are not required. Soft docking requires minimal interaction to align and dock the test head: Docking is secured mostly through the vacuum seal. Hard docking requires mechanically latching the head before setting the vacuum seal.

NOTE Hard docking is recommended, as this procedure places less stress on the vacuum seal than soft docking

Following is an outline of the method of docking the HF test head to a manipulator. More detailed information will be published when available.

1. Ensure the power to the HF test head is turned off.
2. Ensure the test head is horizontal: The chassis is parallel to the floor, and the spring pins of the Split Interface Board point straight up.
3. Ensure the cables from the test head to the mainframe tester are supported. None of the cables need to disconnected.
4. Postion the head as shown in Table 2.39:

Table 2.39: Position HF Test Head for Docking

Required Setup	Distance	Tolerance
X-axis: side to side	4 inches	+ / - 0.05 inches
Y-axis: up and down	25 inches to 52 inches	+ / - 0.05 inches
Z-axis: in and out	4 inches	+ / - 0.05 inches
0X: rotation about X-axis	185 degrees	+ / - 1 degrees gross
0y: rotation about Y-axis	+ / - 0.25 degrees	< 0.010 inches, at 6 inch radius

Table 2.39: Position HF Test Head for Docking (Continued)

Required Setup	Distance	Tolerance
0Z: rotation about Z-axis	(see Planarity)	+ / - 5 degrees gross (see Planarity)
Planarity	+ / - 0.25 degrees	N.A.

For soft docking, ensure the test head is aligned to the DUT interface board (DIB), then activate the vacuum seal. The HF test head has guide posts for alignment.

For hard docking, mechanically latch the manipulator to the test head, then activate the vacuum seal.

Undocking Test Head From Prober / Handler

Following is an outline of undocking the test head from the prober (or handler). Additional information will be published when available.

1. Ensure the power to the test head is turned off.
2. Disengage the vacuum seal.
3. Unlock the mechanical latches.